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FINAL REPORT

APRIL 1965

DESIGN AND DEVELOPMENT OF SOLID STATE IMAGE CONVERTER FOR SPACE VEHICLES

Electronics Laboratory
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Syracuse, New York

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Contract: NAS8-5116

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NASA
HUNTSVILLE, ALABAMA

GENERAL ELECTRIC

HEAVY MILITARY ELECTRONICS DEPARTMENT
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ABSTRACT

This report describes the work performed under contract No. NAS 8-5116 by the Electronics Laboratory of the General Electric Company in Syracuse, New York, during the period 1 June 1963 through 30 April 1965 for the George C. Marshall Space Flight Center, NASA, Huntsville, Alabama. The report covers work performed during a contract initiating on 1 June 1963, and a continuation initiating on 1 May 1964.

Analytical and experimental approaches to determine the feasibility of a solid state image detector are reported. During this program, work has been performed in the areas of:

I. Scanning
   - A. Delay Lines
   - B. Microelectronics

II. Image Sensor Matrix Analysis

III. Device Fabrication
   - A. Nonlinear Elements
   - B. Charge Storage Capacitors
   - C. Photoconductors
   - D. Matrix Fabrication

IV. System Analysis and Limitations.

Work performed in a prior contract is contained in the final report for that program phase and is included as an appendix.

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I. INTRODUCTION

A. IMAGE CONVERTER SYSTEM CONCEPT AND OBJECTIVES

The search for a new concept in image sensing which would eliminate the electron beam, glass envelope, and magnetic deflection coils has led to the device that is presented and analyzed here. Current and projected needs of spacecraft instrumentation have led to the conclusion that a solid state image sensor would have significant areas of application. For this reason, this project has had as its objective, the investigation of circuit and component requirements to achieve an operating system comparable to a vidicon in operational characteristics.

The basic image converter concept is illustrated in the block diagram of Figure 1. It consists of a two-dimensional photosensitive area, with an interconnecting matrix, row and column matrix drivers, and associated syncronizing and scanning control circuitry. The input image is focused on this planar matrix and a signal voltage is produced at the converter output terminals. This voltage, as a function of time, represents a spacial distribution of light intensity over the image area and is processed for viewing using conventional television techniques and circuits. The scanning of the image area is controlled by a common synchronizing source, which regulates both drivers attached to the matrix rows and columns.

The defined system is found to consist of two major areas, the scanning process, and the image sensing process. These areas of development are not independent of each other as is shown explicitly in the system circuit analysis, and thus have been developed in parallel throughout the project.

B. SUMMARY OF PROJECT

The program entitled, "Design and Development of a Solid State Image Converter," (NAS8-5116) was initiated in July 1962. During the initial nine month program, a variety of scanning and image detecting schemes were evaluated from circuit consideration, and the basic feasibility was established.

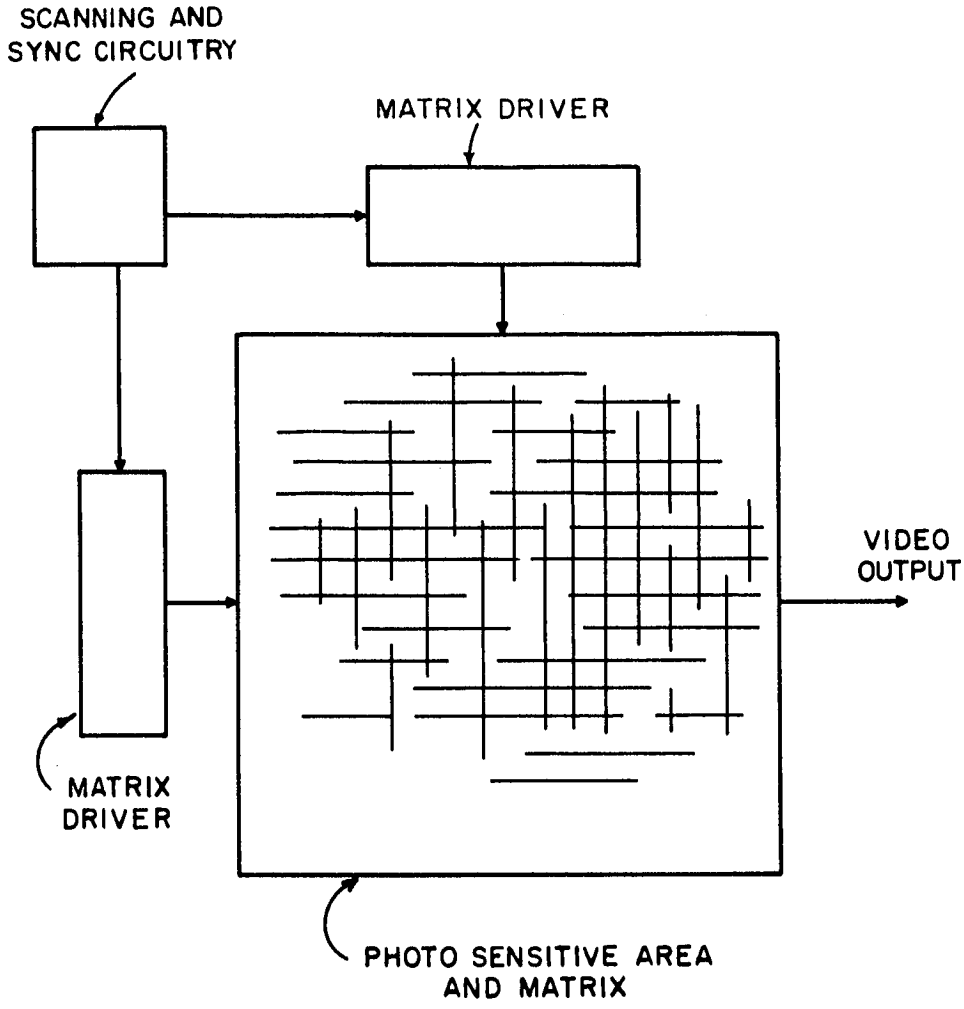


Figure 1. Image Converter Block Diagram

(Results of this program phase were documented in a final report dated May 1963. For the sake of overall program completeness, this report is included as an appendix.)

Following the first phase a continuation program was formulated to fabricate and demonstrate an individual component module of the image detecting matrix. Under this program a 3 x 3 operating matrix was fabricated from individual photoconductors and diodes, and driven by operating delay lines. Test results conformed qualitatively to that predicted by the system analysis.

The third and current phase of the project has had as its goals the refinement of the overall system to conform with restriction imposed by device fabrication requirements. To meet these requirements, a modified image sensing technique and a new implementation of the scanning system were incorporated into the design concept. Device fabrication at a density of 50 lines per inch was successfully accomplished, although additional development was found to be necessary to integrate the several components into a single structure.

C. MAJOR CONCLUSIONS

Results of the refined circuit analysis and device fabrication study during this phase of the project support the previous conclusions of a potentially successful image converter matrix, although at a somewhat reduced resolution capability than the specified 600-800 lines. However, by proper system utilization of the calculated realizable matrix size, the complete goals can be met. In addition, a number of unique modes of operation are obtained that would not be available to conventional vidicon systems.

In this report, the major areas of description are the circuit and system analysis of the image sensor matrix, a discussion of the scanning techniques considered in the program, and a description of the materials and devices efforts to achieve the goal of this phase; namely a 30 x 30 integrated structure at a density of 50 lines per inch.

Limitations of the design goals and areas of required development are specified.

II. SCANNING

A. INTRODUCTION

The image sensor matrix must receive the proper voltage drive pulses to switch the isolation diodes and to generate a current that is proportional to illumination. These voltages must be commutated continuously from element to element in a regular sequence to form a video signal compatible with the display. Two schemes have been developed to drive and scan the matrix. The first to be discussed uses tapped piezoelectric ceramic delay lines. This method is a natural outgrowth of the development pursued during the early phases of the contract with intersecting acoustic waves on a continuous ceramic sheet (see Final Report, May 1963, Appendix A). The second approach uses solid state microelectronic components to obtain driving and timing voltages. The relative advantages of this system compared to delay line scanning have been studied during the last phase of the contract and are discussed below.

B. DELAY LINES

Acoustic delay lines offer the capability of combining both the functions of drive power generation and matrix commutation in a single unit with the expectation of achieving a very simple scanning structure. This scanning scheme has received extensive development throughout the contract.

Metallic contacts deposited at regular intervals along the length of this piezoelectric sheet are used as drive and output electrodes. A common electrode is deposited on the opposite side. In operation, voltage pulse applied across the drive electrode generates a longitudinal stress wavefront that propagates down the sheet, regenerating voltage pulses as it passes between each pair of output electrode. Figure 2 illustrates such a line and Figure 3 shows a typical output waveshape. Because of the attenuation in the ceramic material, the tap voltages decrease with the distance from the drive electrode, and compensating voltage dividers, shown in the figure, must be employed for equalization.

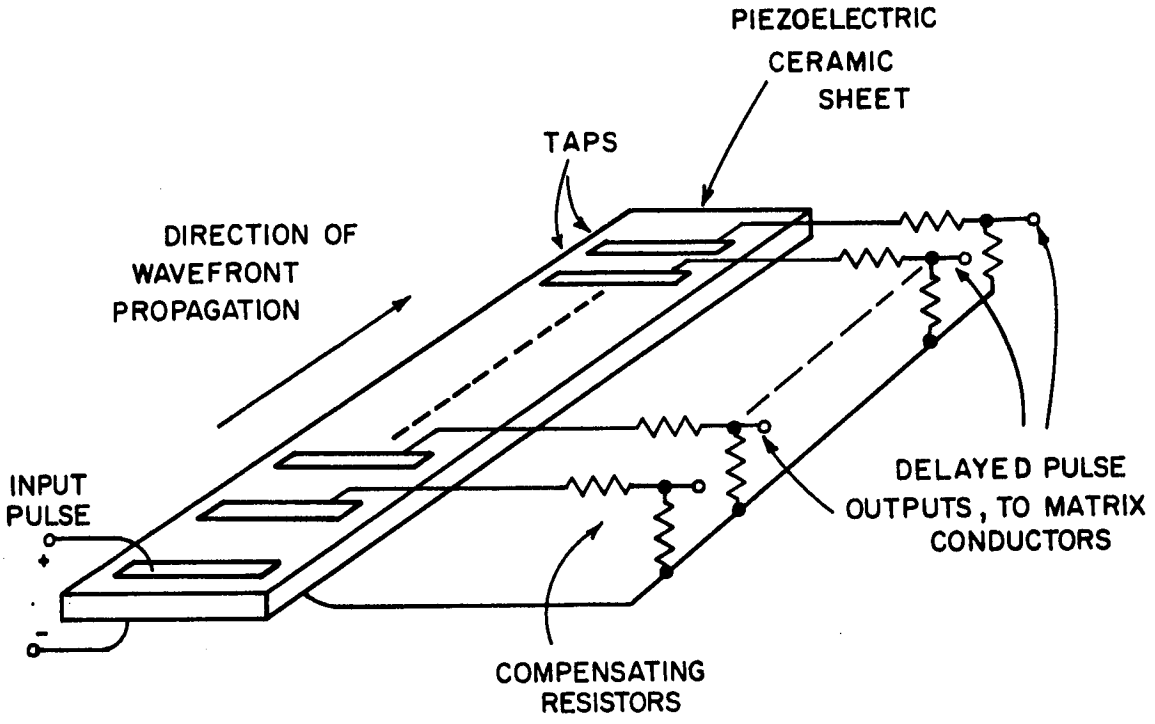
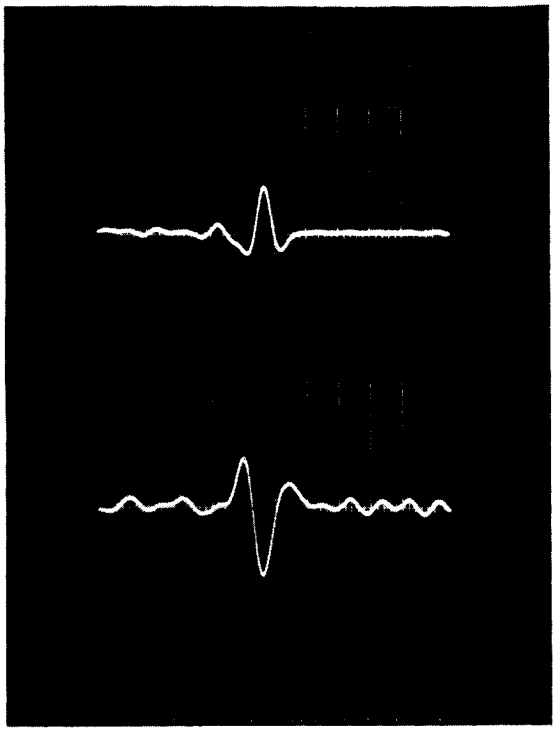


Figure 2. Delay Line Configuration



(a) First Delay Line, with Positive Output Voltage

(b) Second Delay Line, Negative Output

(0.5 ms/cm and 0.25 v/cm)

Figure 3. Delay Line Output Waveforms

Acoustic propagation velocities are utilized so that delay line lengths of a few inches correspond to tens of microseconds of total delay (typical ceramic materials have delays equal to 7 μsec/inch.) The delay time between the tap outputs is then precisely equal to the distance between them divided by the acoustic wavefront velocity. A damping material, not shown in the figure, is added to the edges to absorb the incident waves and prevent reflections within the line.

The tap impedance is largely capacitive, being a function of the ceramic thickness and dielectric constant, and the electrode area. The delay line thickness is a compromise between conflicting requirements; increasing the thickness results in increased mechanical stability and decreased attenuation, but also intorduces dispersive modes at the higher frequencies. The compensating resistors, in addition to adjusting the output voltage, also prevent the accumulation of charge on the output voltage taps. These specialized problems associated with delay line design and fabrication are discussed in more detail in the following sections.

1. System Operation

Two delay lines are used with the image converter matrix, one set of taps attached to the X conductors and the other set to the Y conductors. Coincidence of two pulses at a given intersection governs the selection of the intersection element, using the nonlinear characteristics of the semiconductor diode. The typical forward conduction characteristic is shown in Figure 4. The current I_d is an exponential function of the voltage, V_d, and therefore increases rapidly as V_d is increased. Each diode connected in series with a low resistance photoconductor element, is therefore capable of controlling the current flow through the photoconductor, depending upon the voltage appearing across the junction.

Upon interrogation, a voltage equal to 2V (temporarily neglecting series voltage drops) will appear across the indicated intersection. However, a voltage of only V will appear across those elements (hereafter called primary elements) directly connected to these two particular conductors. Also, no voltage will appear across the remaining elements (to be called secondary

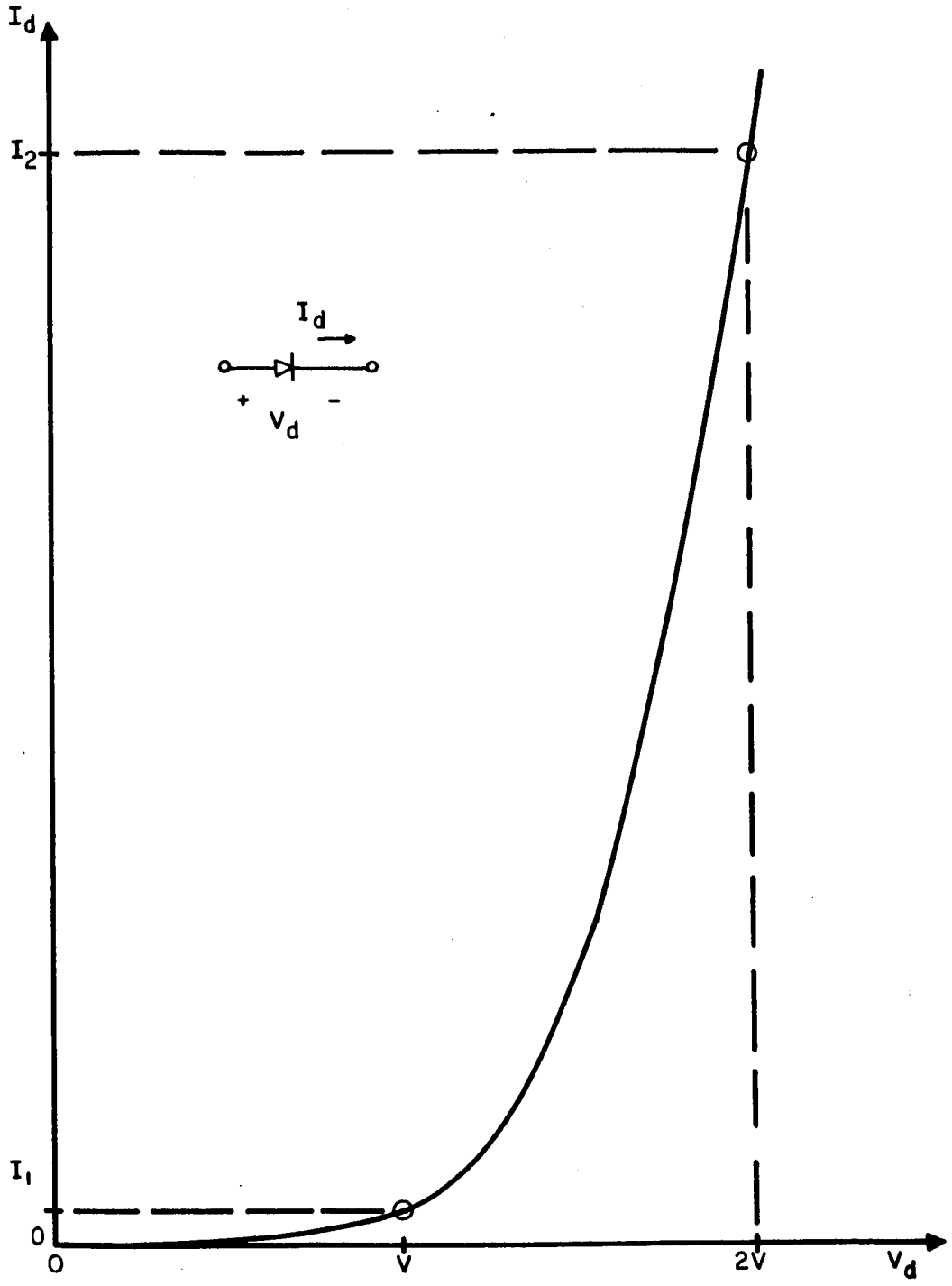


Figure 4. Semiconductor Diode Characteristic

elements) not connected to these conductors, but associated with conductors attached to "off" sources. Because the voltage V corresponds to the diode characteristic as shown in Figure 4, only the interrogated intersection conducts heavily and the output voltage will be dependent mainly upon the photoconductor resistance of this intersection.

The interconnection of delay lines, photoconductor and diode elements is illustrated schematically in Figure 5. Each delay line output tap is represented by a voltage source in series with an impedance Z_p that includes the voltage compensating resistances as well as the tap capacitance. The load resistor is represented here as the input impedance of the first video amplifier. The pulsed reference source associated with each output tap has a peak value of V volts, but only those two sources associated with the interrogated intersection are "on".

The coincident voltage interrogation described above, functions similarly when the parallel combination of a charge storage capacitor and high resistance photoconductor are used as intersection elements. In this case, the capacitor is recharged only when a voltage, 2V, is applied. The small amounts of charge that the remaining elements of the primary row and column receive do, however, degrade the system performance. This effect is discussed later with the aid of equivalent circuits.

The primary elements' current, however, although small, is additive at the load and will tend to mask the lower level signal currents. This situation becomes more critical as the size of the matrix is increased and more elements are added. Therefore, one important design criterion is a high ratio between the currents I_1 and I_2 shown and defined in Figure 4.

Under dc conditions, the current I_1 can be very low. When the diode is pulsed in the forward direction, however, the current I_1 becomes substantially larger due to the diode junction capacitance. Capacitances of a few picofarads, measured at zero bias voltage, have been obtained with the present diodes in use. A capacitance of 1.0 pf operated at 1.0 mc has a capacitive reactance of approximately 160K ohms. The logarithmic curve of Figure 6 shows an exponential diode characteristic with 100, 1K, and 1000 ohms series

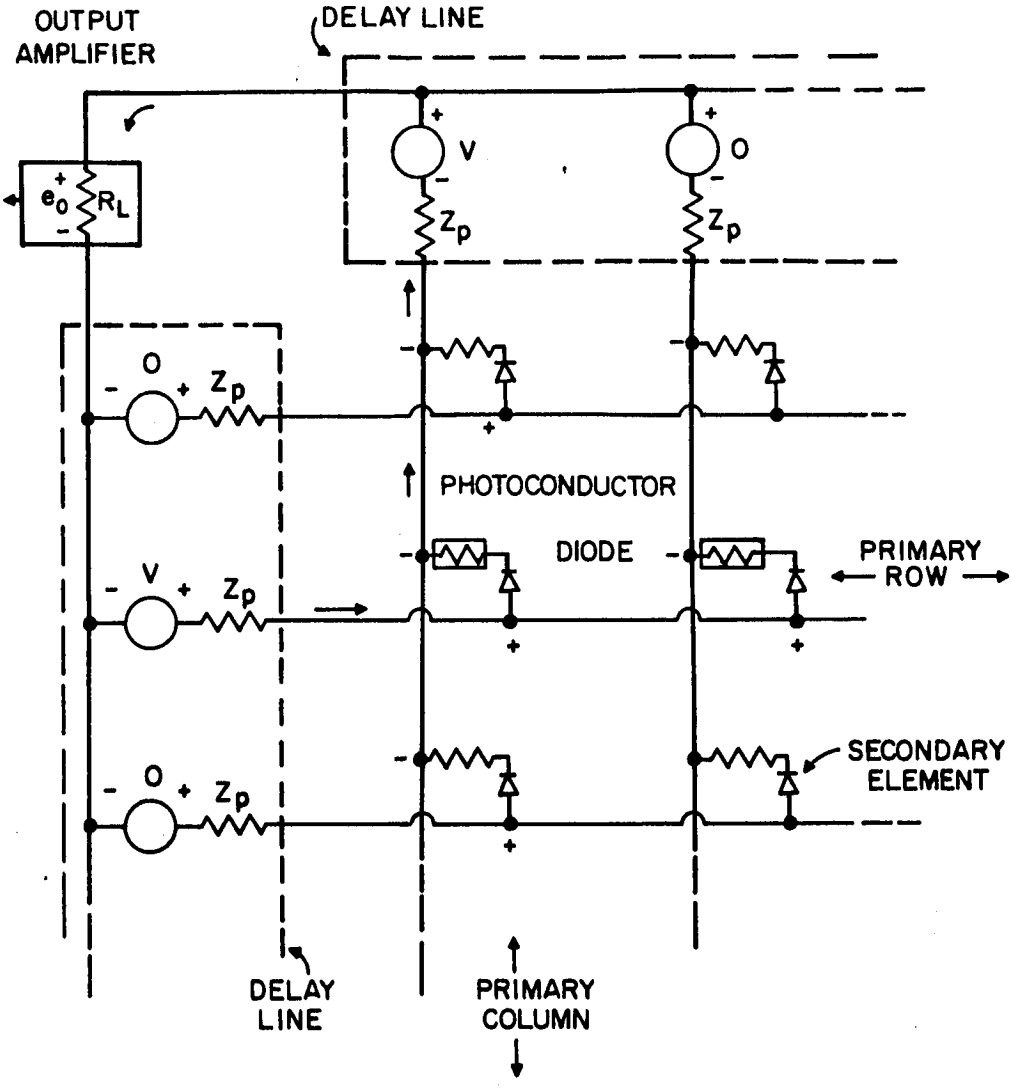


Figure 5. Image Converter Section - Schematic Diagram

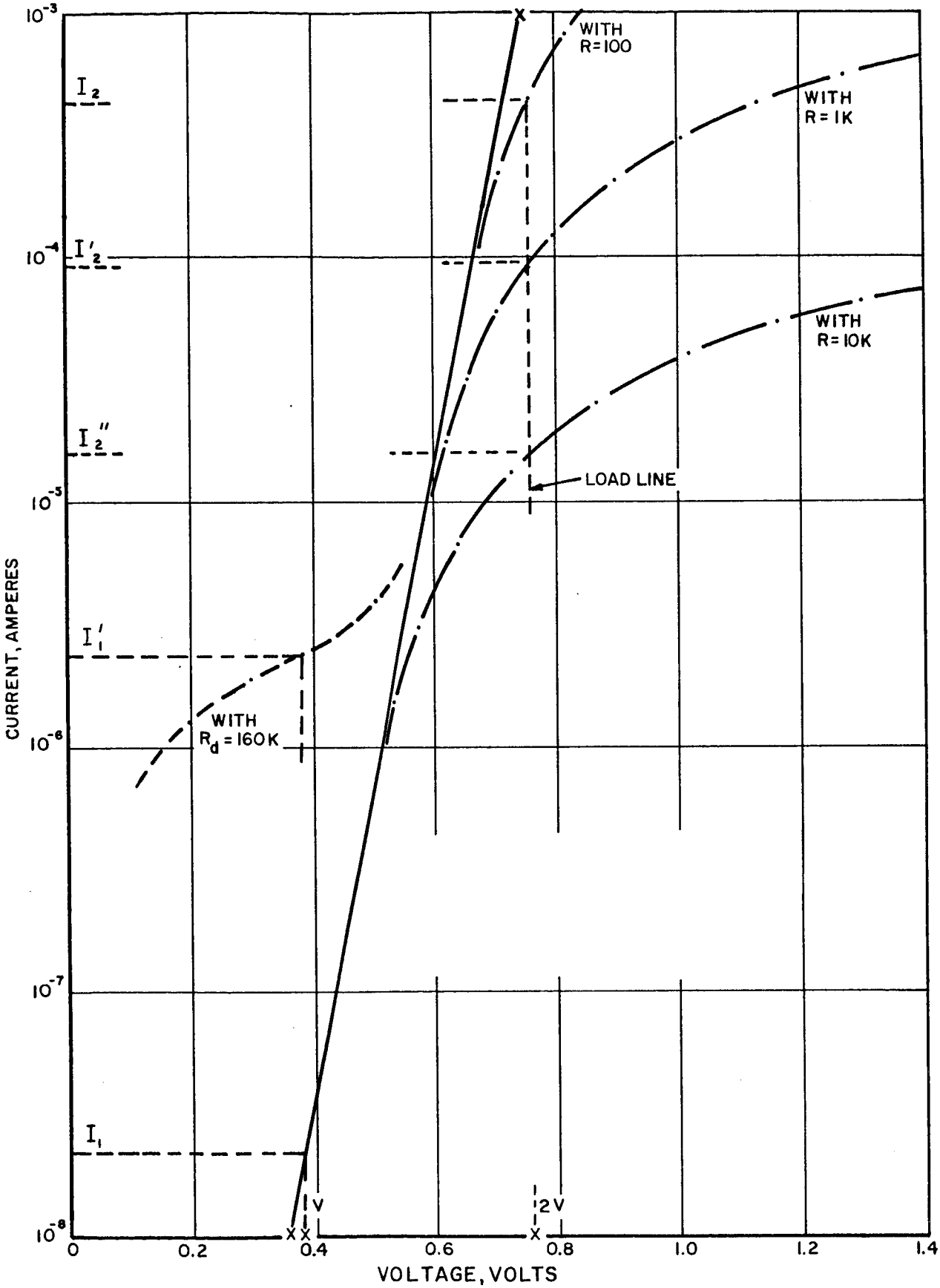


Figure 6. Coincident Voltage Selection Characteristics

resistance, and a 160K ohm shunt resistance. With the half-select voltage, V, applied, the current I_1' is approximately two orders of magnitude higher than I_1. The currents I_2, I_2^1 and I_2^{11} flow when the full select voltage, 2V, is applied.

The capacitance of a given diode is an exponential function of the difference between the applied voltage and the bandgap voltage and, therefore, increases with applied forward bias. Reverse bias of noninterrogated elements is an effective method available for reducing this capacitance.

2. Matrix Scanning

The acoustic velocities in piezoelectric ceramic are essentially constant and cannot be adjusted over a wide range, regardless of the mode selected. Both of the required delay lines must therefore have the same delay. For the matrix interconnection shown in Figure 5, a diagonal scan pattern will result. Consequently, a 90° orthogonal interconnection technique was developed early in the contract and is shown in the first final report (appendix A). Proper transformations of the diagonal rows and columns resulted in a tap requirement approaching one half the number of lines. This is illustrated in Figure 7. A further improvement was made by transforming of the matrix to a 45° interconnection technique, illustrated by the 4 x 4 matrix of Figure 8. The proper timing of one pulse input with respect to the other will allow each line shown to be selected and scanned from left to right. One output tap per line is required for each matrix row and column.

This scanning configuration is an improvement over the previous schemes, where in order to prevent interactions among the delay line pulses, nearly half of the intersections are unused. These potential interactions exist because two pulses are required on each line simultaneously in order to scan the matrix.

Figure 8 also illustrates the electrical connection of the two delay lines to the matrix. Only one delay line common electrode is grounded; the other floats electrically above ground at the signal output potential. This

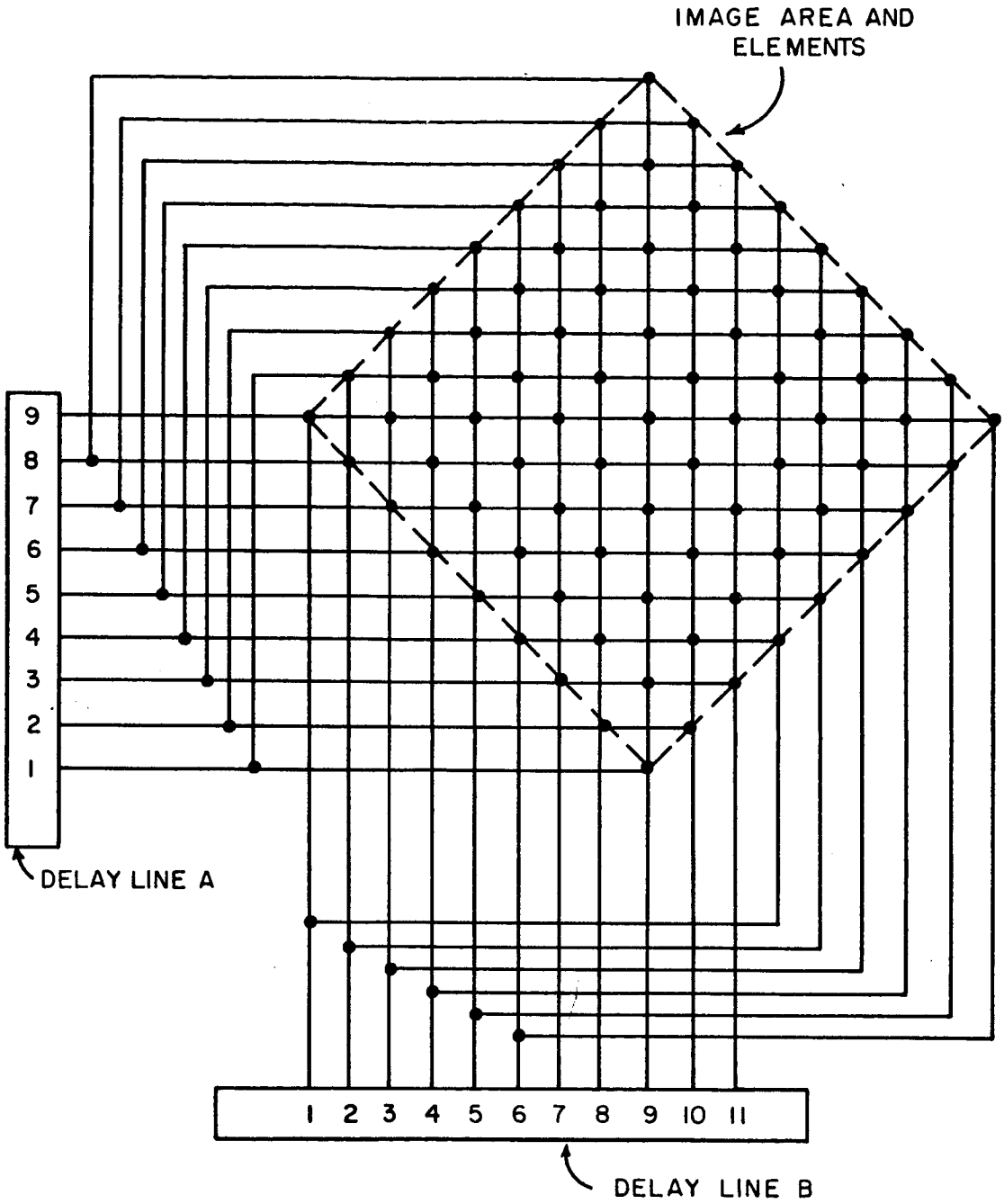


Figure 7. 9 x 9 Matrix Connection Diagram

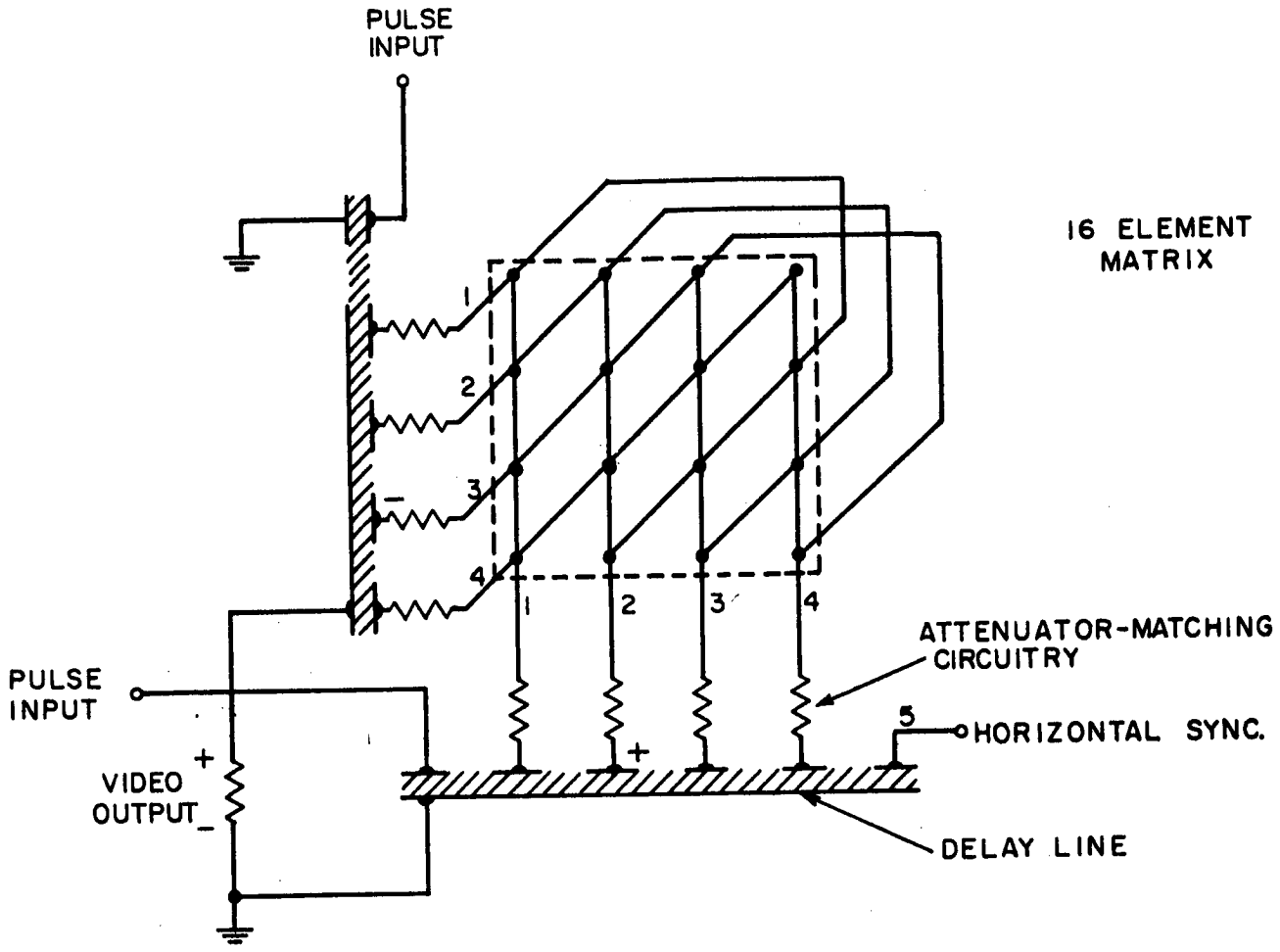


Figure 8. Tapped Delay Line Scanning

This latter line, however, is driven from a grounded pulse source by using an isolated pair of drive electrodes, as shown. In this scheme, the matrix array fabrication is simplified and horizontal blanking signals can be obtained directly from the last tap of the grounded line, as shown. The tap output pulses can also be used to retrigger the driving pulse generators to obtain a continuous scan.

A block diagram of the delay line self-triggering circuits required is illustrated in Figure 9. Both trigger electrodes are connected to the associated drive pulse generator through a trigger delay, and also through a pulse coincidence detector (logical "and" gate). Two logical "or" gates are used to isolate the two paths and to connect them to the proper pulse generator trigger inputs.

For example, retriggering from tap 4 of the vertical line and tap 5 of the horizontal line will result in a scan sequence from top to bottom in Figure 8.

Normally, the trigger electrode outputs appear at different, apparently unrelated times. Once each frame time, however, they coincide, initiating a pulse in the center circuitry. The "and" gate retriggers both drive pulse generators at the same instance, thereby preventing a change in position of one pulse with respect to the other, due to small differences in sync loop delays; and assuring proper registration of the delay line tap outputs. The small added delay in both trigger amplifiers assures that the "and" gate output will trigger the pulse generators at coincidence.

Incorporating interlace scanning is accomplished simply by adding an additional time delay or extra tap, onto the horizontal delay line. In fact, the scanner will interlace every jth row by adding j additional taps.

The driver pulse generators can also be synchronized by a second method, employing a clock signal, that has a number of advantages over the self triggering method. The clock signal period is set equal to the time between successive delay line output pulses. This signal is used to derive two separate pulse signals of lower repetition rate to trigger the drive pulse

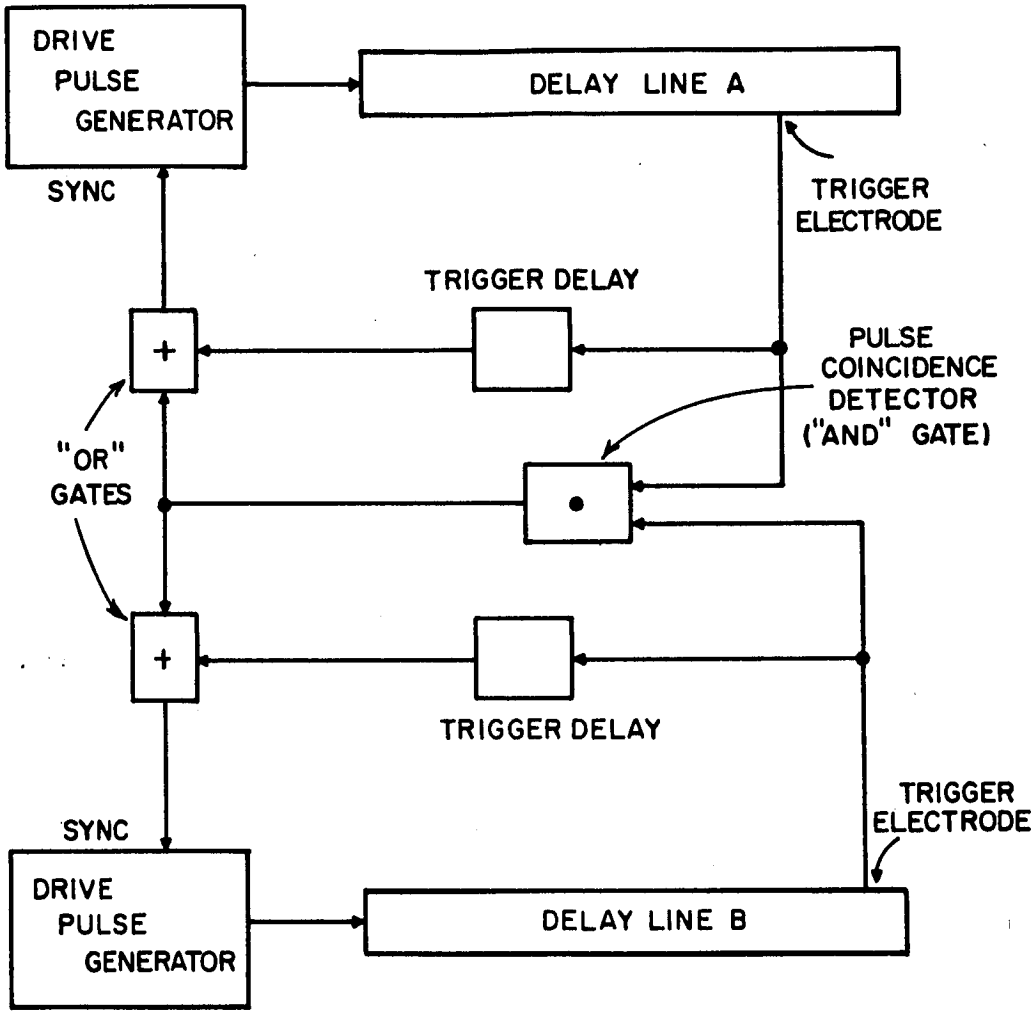


Figure 9. Stabilization and Synchronization Circuitry

generators. Figure 10 shows the block diagram of the timing circuitry used for the 9 x 9 model. Two four stage counters with feedback are required to obtain the 1:9 and 1:10 pulse output/input ratios desired. The 1:9 output triggers the delay line corresponding to line 1 in Figure 8; the 1:10 output triggers the horizontal delay line, 2. The horizontal sync pulse is identical to the 1:10 trigger output. One 2- input gate is used to obtain a vertical sync pulse on the coincidence of the 1:9 and 1:10 pulse outputs, that occurs once each frame. Another 2 input gate is used to inhibit a portion of the 1:10 output pulse.

This triggering method has been incorporated into the demonstration model because of its stability and ease of adjustment. The clock generator is self-starting and its frequency can be adjusted easily. This signal is available also for strobing the output video for further video processing, such as sample and hold.

3. Delay Line Design

a. Materials

Two highly efficient piezoelectric ceramics have been used as delay media in this program.

During the early portions of the program, delay lines were fabricated from Gulton G527 0.005 inch sheet ceramic. This material is characterized by a high electromechanical coupling coefficient (.35), a high dielectric constant (1500) and a low mechanical quality factor (75). The first two characteristics imply a relatively high output voltage at each tap at a low output impedance. These are desirable for the present application. However, the low mechanical quality factor is reflected as a rapid decrease in the acoustic stress wave as it propagates along the sheet. This is undesirable since the delay line output voltage should be as constant as possible from tap to tap in order to drive the sensor array. For these reasons, it was felt desirable to use a different ceramic for the delay line material. A General Electric ceramic, type 427AA, was selected. This ceramic is a modified lead zirconate titanate characterized by a high coupling coefficient

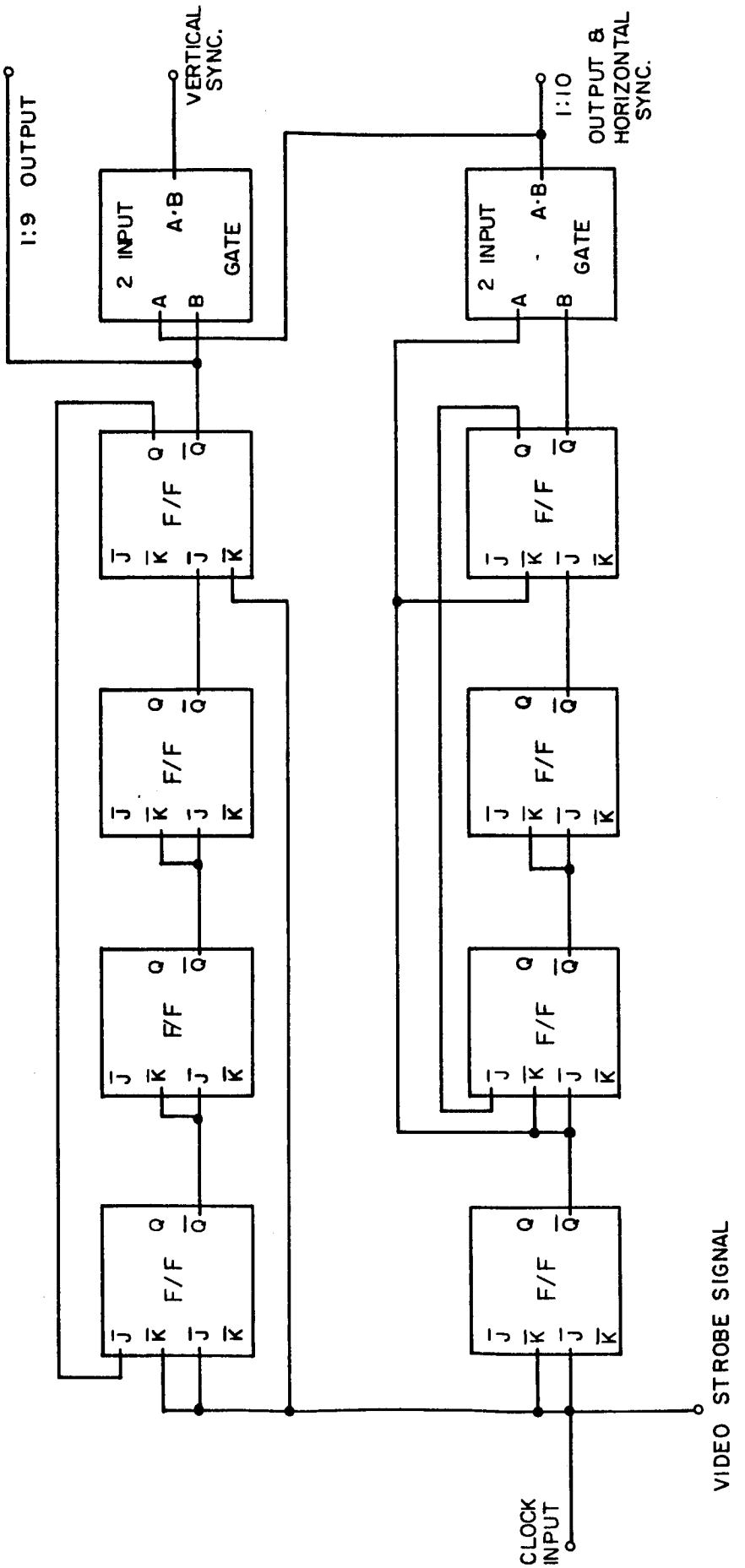


Figure 10. Delay Line Timing Circuitry

(.30) a high dielectric constant (1000) and a high mechanical quality factor (600). Most of the results given in this report were obtained using this ceramic. Normally the delay lines were fabricated from sheets 1 inch wide, 3 inches long, and 0.010 inches thick. A number of lines, fabricated from a barium titanate sheet, General Electric type 235, were not successful.

The ceramic sheet thickness must be no greater than a half wavelength of the highest acoustical frequencies excited to prevent the propagation of dispersive modes. Thin sheets of 5-10 mil thickness, have been required. Such sheets are brittle and require careful handling during processing. However, a properly mounted ceramic sheet is capable of withstanding large shocks and vibration, without fracture, as discussed further below.

b. Electrodes

Two electroding procedures have been used in this program to obtain a low resistance, mechanically stable contact to the ceramic surface that does not interfere with the acoustic wave propagation. The first method consists of sputtering metals through masks on the ceramic surface. Successive layers of nichrome, gold, and copper were applied. A thin nichrome layer assured good electromechanical coupling, and a thin layer of gold was required for good adherence of the heavier layer of low resistance copper. The metal masks and sputtering holder used are shown in Figure 11. The common electrode was applied to the opposite side without masking.

Although the mask openings were carefully machined, the sputtered electrodes themselves were of varying widths, due to warpage of the 5 mil ceramic sheets. Because the tap output voltage is maximum only when all taps are of equal width, a more accurate electroding method was studied. This method involves the electroless deposition of metal from solution through photoresist masks on the surface of the ceramic sheet. Both copper and nickel deposition has been successful. Figure 12 shows the various masks used. Photoresist is first removed from those areas where metal is desired, and then the excess is removed after deposition. These electrodes, applied to the GE 427 AA ceramic, were largely successful. Some samples had rather

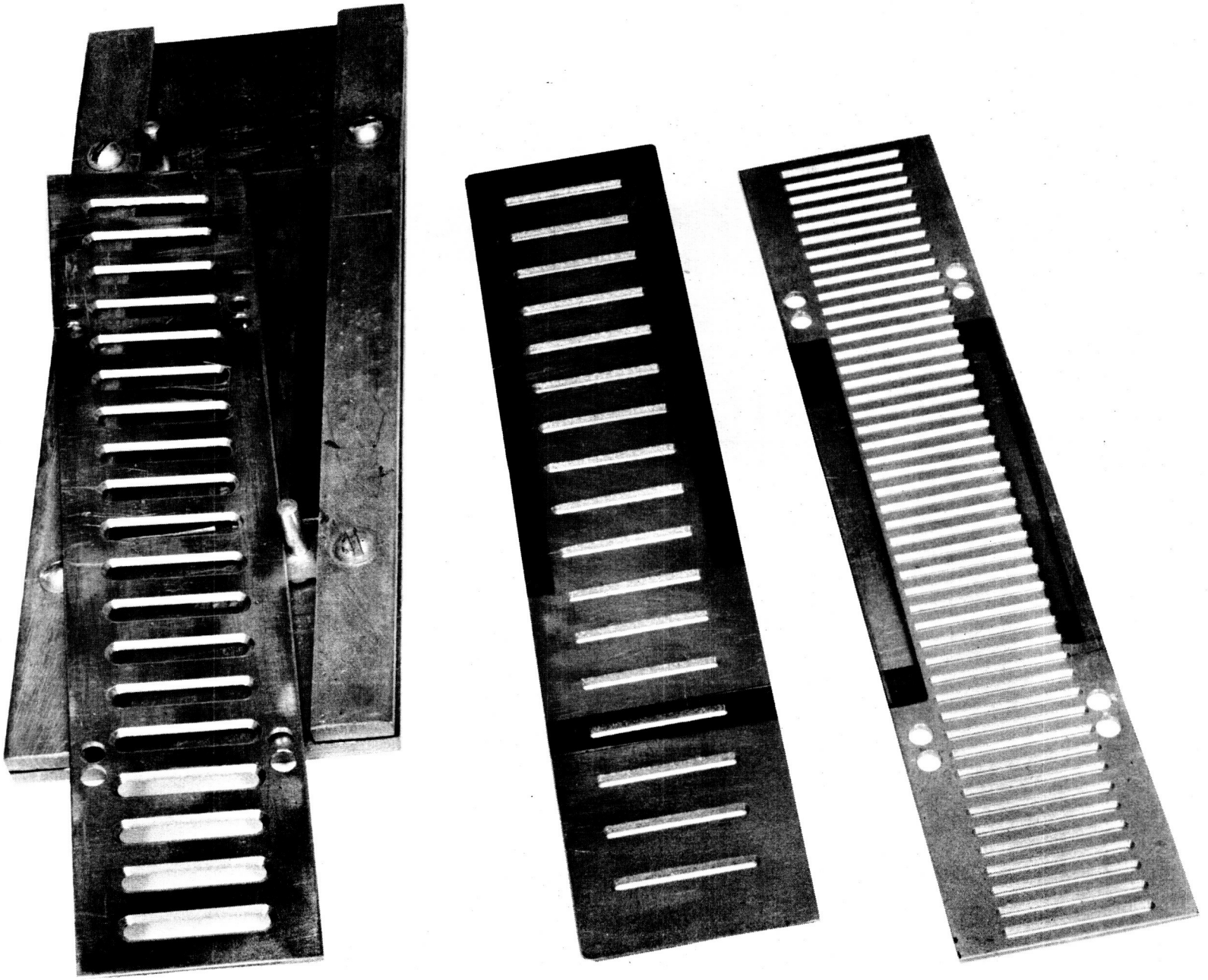


Figure 11. Delay Line Electrode Masks

(a.) 120 MIL CENTERS (b.) 60 MIL CENTERS

TOP ELECTRODES

(c.) 30 MIL DRIVE TAP (d.) 180 MIL DRIVE TAP

BOTTOM ELECTRODES

Figure 12. Delay Line Deposition Masks

high resistance electrodes (200-2000 ohms), due to abnormally thin metal deposition. This problem was thought to be due to improper use of the required sensitizer. Some lines were temporarily repaired using air dry silver paste, applied over the metal with a brush and successfully operated.

Leads of 2 mil wire are attached to the electrodes with silver paste, conducting epoxy, or soldering. These leads are mechanically quite stable as shown by the results of the shock and vibration tests.

c. Reflections/Damping

Stress wave reflections from the edges of the ceramic and from the metal taps added to the tap signals in the form of noise, and must be minimized to prevent unwanted matrix signals. A number of edge doping materials have been applied to absorb the reflections. The compound that was most successful when used with the Gulton ceramic is an acoustic sound deadener, consisting of asbestos in a binder. The more recent delay lines using GE427AA ceramic, require more damping because of the increased quality factor.

For this reason, a larger ceramic area was left between the electrode area and the sheet edges, to allow the application of more damping material. Rubber stripping compound and glass fiber tape were applied to the line edges. These materials, although normally effective, did not reduce reflections sufficiently.

Relative success, however, was achieved by scalloping the edges of the line to break up and disperse the incident wavefront. Scalloping was accomplished simply by fracturing small pieces from the edges of the ceramic sheet.

Figure 13 shows a number of experimental lines that have been fabricated and tested, some with the various damping methods discussed above.

The two delay lines at the upper left, mounted on printed circuit boards, are Gulton ceramic with sputtered nichrome electrodes. The asbestos acoustic deadener is the damping material. The two long lines directly below are General Electric 235 ceramic with 100 mil wide sputtered electrodes. Asbestos damping was applied to these lines. The five lines remaining are fabricated from General Electric 427AA ceramic. The short

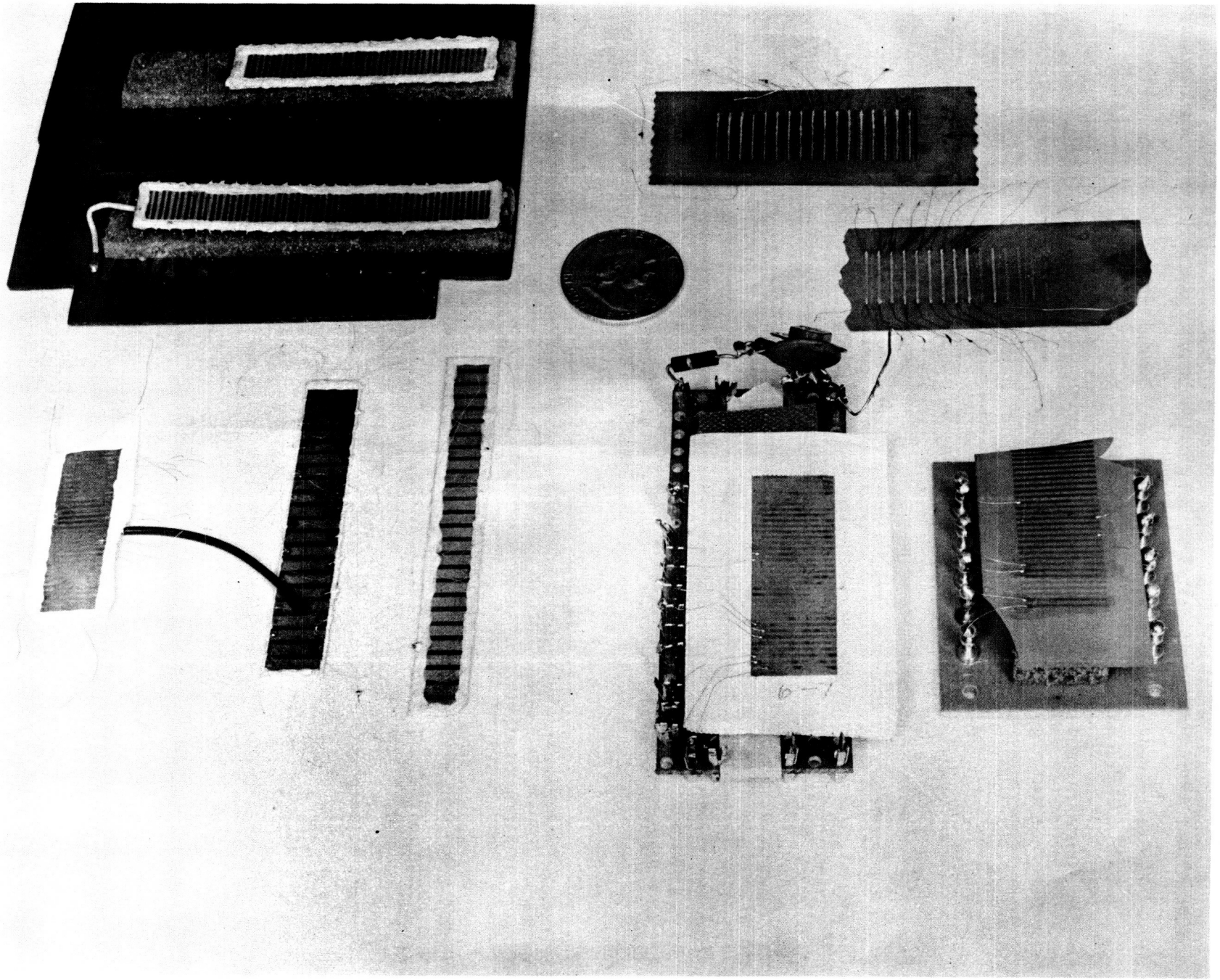


Figure 13. Delay Lines

line at the left is damped with rubber stripping compound. The electrodes are electrodeposited copper, with a 60 mil center-to-center spacing. The electrodes of the delay lines at the upper right have been retouched with silver paste. The edges of the upper line have been scalloped. Glass tape is the dampener used on the line at the lower right. The line at the far right has no damping, but illustrates the isolated drive electrode configuration.

A new electrode placement was attempted to eliminate the large reflection from the edge parallel to and nearest the drive electrode. The electrode pattern was placed on the ceramic so that the edge of the drive electrode was flush with the edge of the sheet. The reflected wave then contributes to the forward wave, giving a slight increase in output voltage. The increase was somewhat less than expected, and there is some tendency for the waveform to distort as it propagates down the line. The output waveshapes changes in many of the lines from positive pulses to negative pulses or to double pulses of reduced amplitude. Propagation of a single positive pulse along the entire line has been successful in some lines; these lines have been used in the 9 x 9 breadboard model.

Waveform distortion of this type exists to some extent in all of the lines fabricated. Some interference is thought to be due to the electrical short circuit presented to the wave across the width of each output tap. To reduce this effect, alternate taps were eliminated from some of the recent lines fabricated. Figure 12 has shown both the old and the new tap spacing.

d. Drive Pulse Generator Isolation

The image converter circuitry of Figure 8 requires that one delay line common electrode be isolated from ground. It is convenient, however, to drive the line from a grounded pulse generator. Therefore, a split electrode configuration is used, as illustrated in Figure 12. This method was used with success on the Gulton ceramic lines fabricated earlier in the program. When the high Q, GE427AA ceramic was used, however, a noise signal was present across the gap. The noise waveform is irregular and of sufficient magnitude to mask the video output, which is taken across the same two terminals.

Any acoustic wave traversing the gap whether due to the main acoustic wavefront or individual reflections from the output electrodes, contributes to the noise.

A number of solutions of this problem were proposed. The gap between the common electrodes was increased, and output taps above the gap removed, with only a slight reduction in noise. A line with one common electrode, and driven from a pulse generator isolated with a pulse transformer, eliminated the acoustic noise, but exhibited capacitive coupling of a differentiated drive pulse into the video signal.

A new readout circuit was studied briefly, that allows both lines to be grounded. The video output is obtained by diode coupling from each top of one delay line to a common load resistor. The scheme functioned well in a single element interrogation test, but is somewhat sensitive to voltage variations, since the video output is proportional to the amount of voltage unbalance that results from a given interrogation.

The most successful solution to the problem involved a detailed study of the noise mechanism. Initially, the delay lines were fabricated by uniformly polarizing the ceramic sheet through its thickness before the electrodes were applied. Because of this polarization, a certain amount of electromechanical coupling existed between the two electrodes, which would cause a voltage generation across the electrodes in response to acoustic stress. The entire delay line was, therefore, depolarized by heating it above its Curie temperature and repolarizing only between the electrodes used. The video noise was reduced nearly an order of magnitude, along with a 30% reduction in the output voltage. Also, the propagation velocity was decreased approximately 3% due to the nonuniform poling. To insure pulse coincidence, the normally grounded delay line was repoled in the same manner. Propagation velocities within 1% resulted, which were sufficient for operation of the 9 x 9 model. This would, however, require more detailed material, electroding, and polarization if a greater number of taps were to be used.

e. Shear Mode Delay Lines

Most of the delay lines fabricated and discussed above have used longitudinal waves, whose propagation velocity is approximately 7 μsec/inch. With this mode of propagation, a 9 inch length is required to obtain a delay of 63 μsec, as needed, for conventional television scanning. Although this total delay could be achieved with a number of shorter lines, it is desirable to obtain slower propagation delay lines. Therefore, a limited investigation of the possibility of using shear waves as the acoustic mode of propagation was carried out during this program. The velocity at which these waves propagate is about two thirds that of longitudinal waves and thus would enable the use of shorter delay lines. The study indicated, however, that this method is not practical with the present system.

Piezoelectric excitation and detection of shear waves requires that the ceramic sheet be polarized in a direction perpendicular to the direction of propagation. It was found in practice that it was difficult to achieve this polarization due to the fragility of the thin delay sheet. The large mechanical strains developed during polarization were sufficient to cause fracture of the sheet.

The electroding configuration presently used on longitudinal mode delay lines is desirable because of its ease of fabrication, high capacitance, and the fact that one electrode must be applied for each additional output tap. Unfortunately, all the shear modes that can be excited or detected with this arrangement are dispersive (the delay changes with frequency) and are thus not usable in this application due to severe distortion of the acoustic wave as it propagates through the sheet.

A nondispersive shear mode can be excited and detected by using two electrodes for each tap. These electrodes would be applied to the same surface of the sheet and perpendicular to the direction of propagation. Each electrode pair would be spaced one half acoustic wavelength apart. This arrangement would be more complex to fabricate than the present one and would probably have a lower capacitance than the present technique. Neither of these arrangements was evaluated due to the lack of a suitably polarized ceramic sheet.

f. Matching and Attenuation Pads

Compensating resistor networks are required between the delay line output taps and the matrix conductors to correct the output voltage characteristics of the tapped delay line. Two conditions must be met: 1) Each matrix conductor must receive a voltage pulse of an amplitude, V, to accomplish the coincident selection of a matrix element. 2) Each pulse source must have the same Thevenin source impedance so that each source acts identically under varying matrix impedance conditions due to illumination.

In addition, a resistive path from the tap to the common electrode is required to prevent accumulation of change on the tap. A few thousand ohms resistance is sufficient for the highest pulse repetition rate used. Figure 14 illustrates the decrease in voltage pulse amplitude that is obtained as the distance from the drive tap is increased. The line measured is of GE427AA ceramic, with electrodes on 60 mil centers. When $R = \infty$, no power is taken from the taps, and the voltage decrease is due entirely to internal losses. When $R = |Z|$, the maximum power is taken from each tap. The increased slope is the sum of internal losses and the power removed from each preceding tap. If a large amount of power must be drawn from 30 taps, for example, a voltage adjustment over a range of more than an order of magnitude is required. When small amounts of power are drawn, a characteristic curve between those of Figure 14 is obtained, and less voltage compensation is necessary.

This voltage adjustment and source impedance compensation is accomplished by the use of a resistive pi-network, illustrated in Figure 15. Resistors R_1 and R_2 function as a voltage divider. Resistor R_3 is used to adjust the network for a constant input impedance. Resistor R_3, however, reduces further the voltage available to the matrix under load. The resistor values must, therefore, be chosen together and with a knowledge of the matrix load. The isolating diode is used to minimize reverse currents through noninterrogated elements and inactive taps. Its function will be discussed further with the aid of the equivalent circuit.

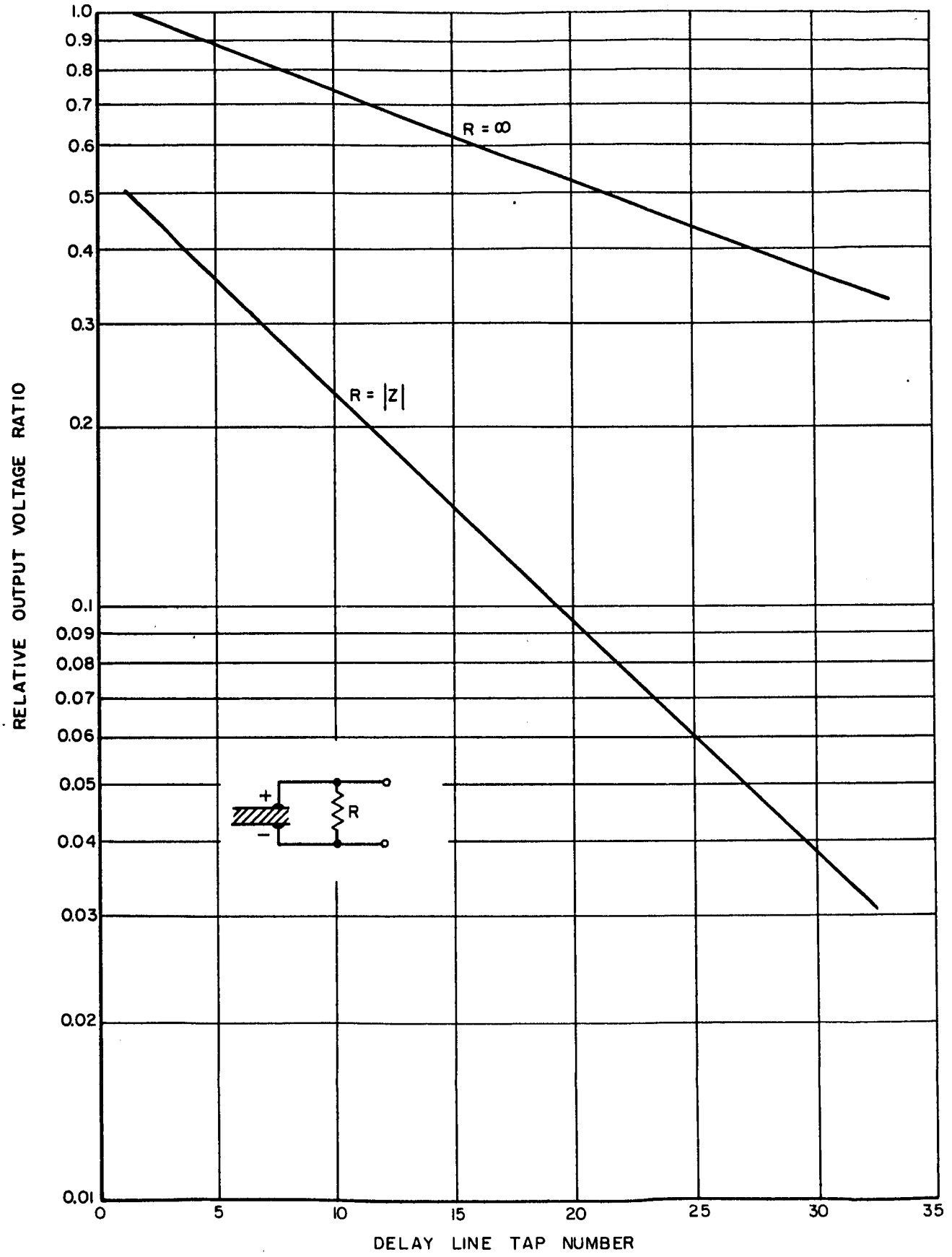


Figure 14. Delay Line Tap Load Conditions

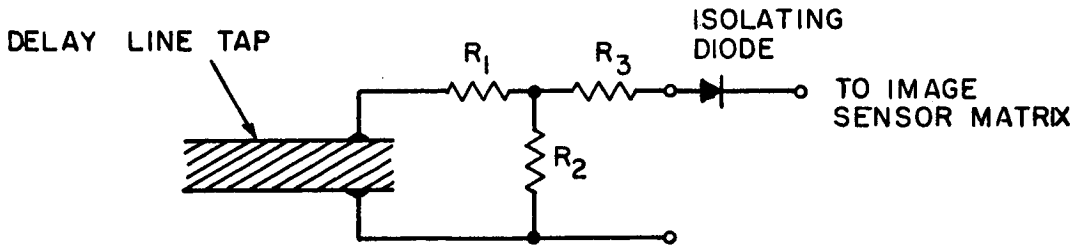


Figure 15. Attenuating and Matching Network

Values of resistance have been calculated for a tap impedance of 330 ohms, a matrix load of 200 ohms, and a total allowed source impedance of 530 ohms. The sum of R_1 and R_2 is chosen to be constant and for these values becomes 1800 ohms. Three cases are tabulated below, for a total network load of 200 + 530 = 730 ohms.

V_{out}/V_{in} (1)	R_1	R_2	R_3	Input (2) Impedance, R_a	Tap (3) Load, R_b
0.744	0 ohms	1800 ohms	253 ohms	532 ohms	637 ohms
0.371	735	1065	0	532	1169
0.107	1470	330	253	532	1717

(1) V_{in} is the voltage across $R_1 + R_2$;
V_{out} is the voltage across $R_3 + R_2$.

(2) R_a is the network and tap impedance, measured at the V_{out} terminals.

(3) R_b is the network and matrix load, measured at the V_{in} terminals.

In each case above (and for all intermediate values) the input impedance R_a remains the same, regardless of the V_{out}/V_{in} ratio. A voltage range of $0.744/0.107 = 6.95$ can be accommodated. These values will compensate the outputs of approximately 30 taps of the delay line of Figure 14 because the load on each tap is from two to five times the tap impedance. The higher V_{out}/V_{in} ratio is used for the last tap, and the lower, for the first tap.

Figure 16 illustrates the electrode and material layout for the thin film deposition of these compensating resistors. The constant value of $R_1 + R_2$ allows an adjustment in resistance ratio to be made simply by changing the electrode position.

g. Delay Line Power Output and Efficiency

Ferroelectric ceramic delay lines are used for two purposes with this image converter. They provide the timing of the sweep, as well as the power to drive the sensor array. It is the purpose of this section to examine the design of the delay lines in terms of their power handling requirements under the following idealized assumptions:

1) The acoustic loss in the delay material is negligible
2) The acoustic wave is confined to the region of the ceramic upon which the electrodes are placed. That is, no reflection or absorption of the acoustic wave occurs at the edges of the delay sheet.
3) Reflections of the acoustic wave at each electrode are negligible.

It is also assumed that a constant fraction α of the incident acoustic wave at each electrode is converted to electrical power. A variable portion of this power may be delivered to the sensor due to resistive padding but this is not relevent to the present discussion. In practice, the parameter α is related to the electromechanical coupling coefficient of the ceramic and the resistive loading on the delay line taps. This loading is here assumed to be substantially constant except for small variations due to changes in sensor illumination.

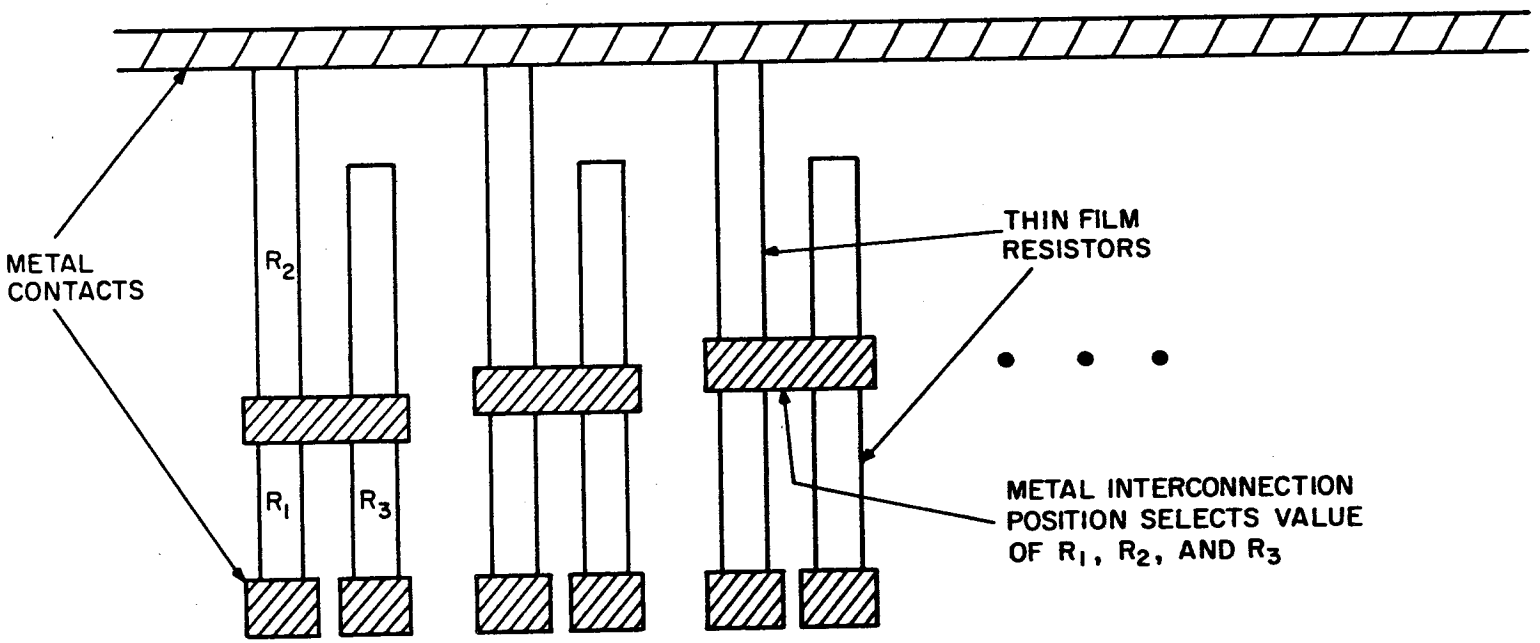


Figure 16. Thin Film Resistors

In the following discussion, the diagram of Figure 2 represents the physical arrangement of the electrodes.

Application of a drive pulse to the drive electrodes results in an acoustic pulse of power P_1 which is incident on electrode 1. At this electrode, an output power $P_{o1} = \alpha P_1$ is coupled out of the delay line. Therefore, the power incident on electrode 2 is given by

$$P_2 = (1 - \alpha) P_1 \quad .$$

Similarly,

$$P_{o2} = \alpha P_2 = \alpha(1 - \alpha) P_1 \quad ,$$

and

$$P_3 = (1-\alpha)^2 P_1 \quad .$$

At the last electrode, i = N, the output power is given by

$$P_{oN} = \alpha (1 - \alpha)^{N-1} P_1$$

so that the input acoustic power required on a per unit output basis is

$$P_1 = 1/\alpha \ (1 - \alpha)^{N-1} \quad .$$

This last expression indicates that for a given N determined by the array sensor, there is a particular value of α that will minimize the acoustic drive required to meet the power requirements at the N^{th} output tap. This in effect balances the inefficiency of output coupling due to a too small value of α against the effect of delivering too large a portion of the available acoustic power in the first few taps due to a too large value of α.

Straightforward minimization of P_1 with respect to α indicates that the desired value is

$$\alpha_o = 1/N \quad .$$

It should be noted that this value will also make the output power at any tap most independent of small changes in loading on the preceding taps. If this condition is satisfied, the per unit input power is given as a function of the number of taps by

$$P_1 = \left(\frac{N}{N-1}\right)^{N-1} \cdot N \approx e \cdot N$$

where the approximation is good for N greater than ten. That is, the required acoustic input power is directly proportional to the number of taps required.

The efficiency of the delay line as a power source can also be estimated bearing in mind the assumptions made earlier.

The delay line efficiency will be defined as

$$\text{Efficiency} = \frac{P_{out}}{P_{in}} = \frac{P_1 \sum_{i=1}^{N} \alpha (1-\alpha)^{i-1}}{P_1}$$

$$= 1 - (1-\alpha)^N$$

Again assuming that

$$\frac{1}{\alpha} = \frac{1}{\alpha_o} = N ,$$

the efficiency is given by

$$\text{Efficiency} = 1 - \left(1 - \frac{1}{N}\right)^N \cong 1 - \frac{1}{e}\left(1 - \frac{1}{N}\right)$$

$$\cong 63\% \quad (N \text{ large}).$$

Since the derivation assumes an input power of P_1 already existing within the line, an additional loss factor due to the coupling coefficient (η) of the drive line must be included. The idealized external efficiency is then

$$\text{Efficiency} \approx \frac{63}{\eta}\ \%$$

The measured line of Figure 14 was used to calculate an actual efficiency, and the comparison between this and the measured efficiency is quite good.

The effective α is obtained from a combination of the actual α and the line losses which are neglected in the formula derivation. This is done by taking the effective voltage output as the voltage difference between the $R = |Z|$ and $R = \infty$ curves. The value of α is then calculated from

$$(1 - \alpha) = \frac{P_{o_M}}{P_{o_{M-1}}}$$

Across the 30 taps of this line, the value of α ranges from .022 to .037.

A calculated efficiency is then obtained from

$$\begin{aligned} \text{Eff} &= 1 - (1 - \alpha)^N \\ &= 1 - (.97)^{30} \\ &= 60\% \end{aligned}$$

Coupling coefficient for the drive line can be calculated from the power ratio of the first top output to the input. This coefficient is about 0.2, thus the calculated efficiency for the line should be 12%. Actual measurement of the output power and efficiency yields a value of 4%

$$\text{Eff} = \frac{\sum_{v=1}^{30} V_{o_j}^2}{V_{in}^2}$$

The discrepancy can be explained by the other loss neglected in the assumptions.

h. Measurement of the Effect of High Acoustic Pressures, Shock and Vibration Upon Compensated Line Output

For this purpose, two ceramic lines were mounted in a standard aluminum coil form can, Millen type 74400. Figure 17 is a photograph of the components, prior to assembly. A foamed polyurethane pad was cut to fit snugly within the can, and sliced lengthwise into three rectangular parallelepipeds. Two were reassembled to contain an aluminum stiffening plate, .015" in thickness, using

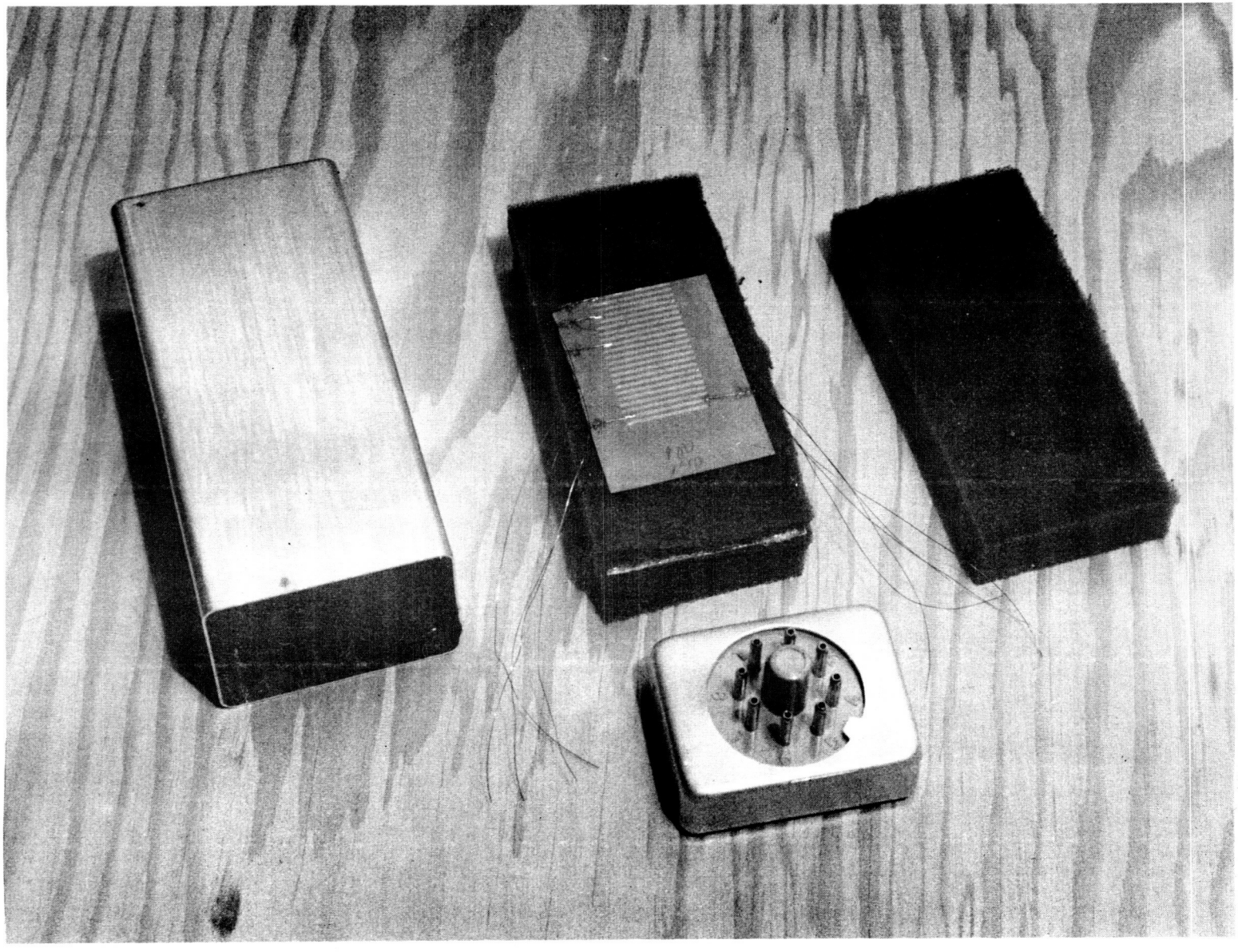


Figure 17. Delay Line Vibration Test Mounting

General Electric RTV-108 silicone rubber adhesive sealant. The RTV was cured at approximately 65°C. The ceramic line was then edge-sealed to the stiffened pad with RTV, and then the top pad was added, again using RTV as a cement. This again was cured. The assembly was then placed within the can, using RTV as a cement between pad and can walls, and cured. The octal header, with leads soldered in place, was then attached with mounting screws and sealed in place with RTV and given a final cure. Two units of this type were prepared.

For reference, an output signal from the ceramic line before mounting was recorded, in Figure 18. After mounting the output was essentially unchanged, as shown in Figure 19. This line was selected from laboratory rejects for the environmental tests, since the tests were expected to be destructive. It should not be regarded as typical in performance, but provides a basis for evaluation of packaging and environmental effects.

A moderately intense sound source was set up in the laboratory, within an enclosure deadened for minimization of acoustic standing waves. The sound source was a University model T-50 tweeter, rated for frequencies from 600 cps to "above audibility" at a program level of 50 watts input power, and a suggested derated level of 5 watts for cw input. This was operated during tests at approximately 6 watts of input power, with cw sine wave excitation from a McIntosh model A-116 power amplifier. The mounted delay line, and a General Radio Type 1555-A Sound Survey Meter were placed in close proximity to the mouth of the tweeter horn, and readings from the sound meter were used as the measure of incident sound intensity. It was found that the 130 db level could not quite be maintained at frequencies above 6000 cps, within the 6 watt limitation, and so the measured microphonic level has been raised to compensate for reduced intensity. The response curve is shown in Figure 20. At frequencies above 13 kcs, it appears that calibration of the sound survey meter may account for the observed rise in microphonic response, since a considerable drop in level for constant drive power was observed. The largest microphonic response

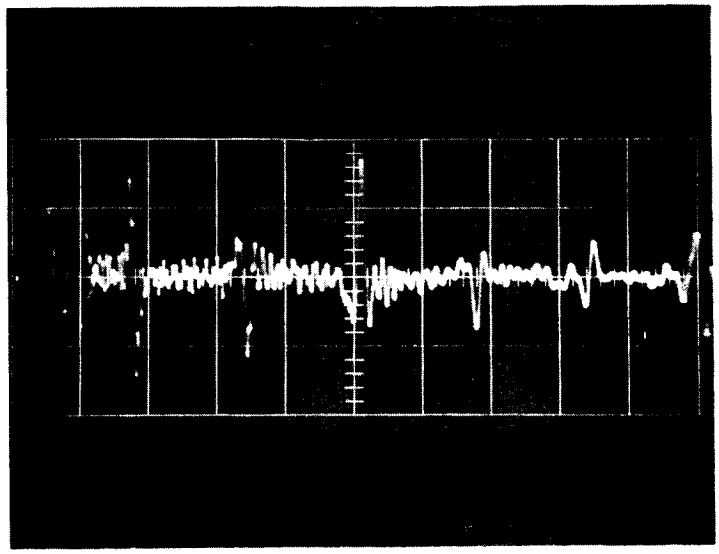


Figure 18. Response of a "Reject" Line, Selected for Environmental Testing, to a Rectangular Voltage Pulse. Sweep Rate is 5 Microseconds per Division.

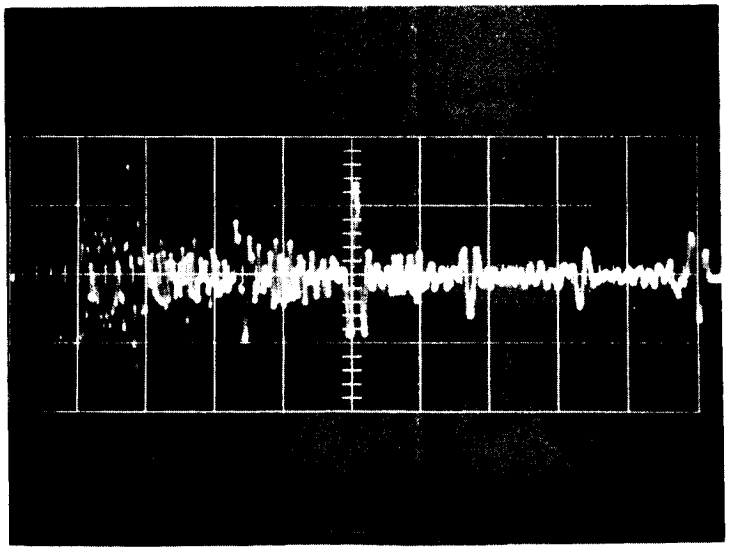


Figure 19. Response of the Environmental Test Line in its Mounting.

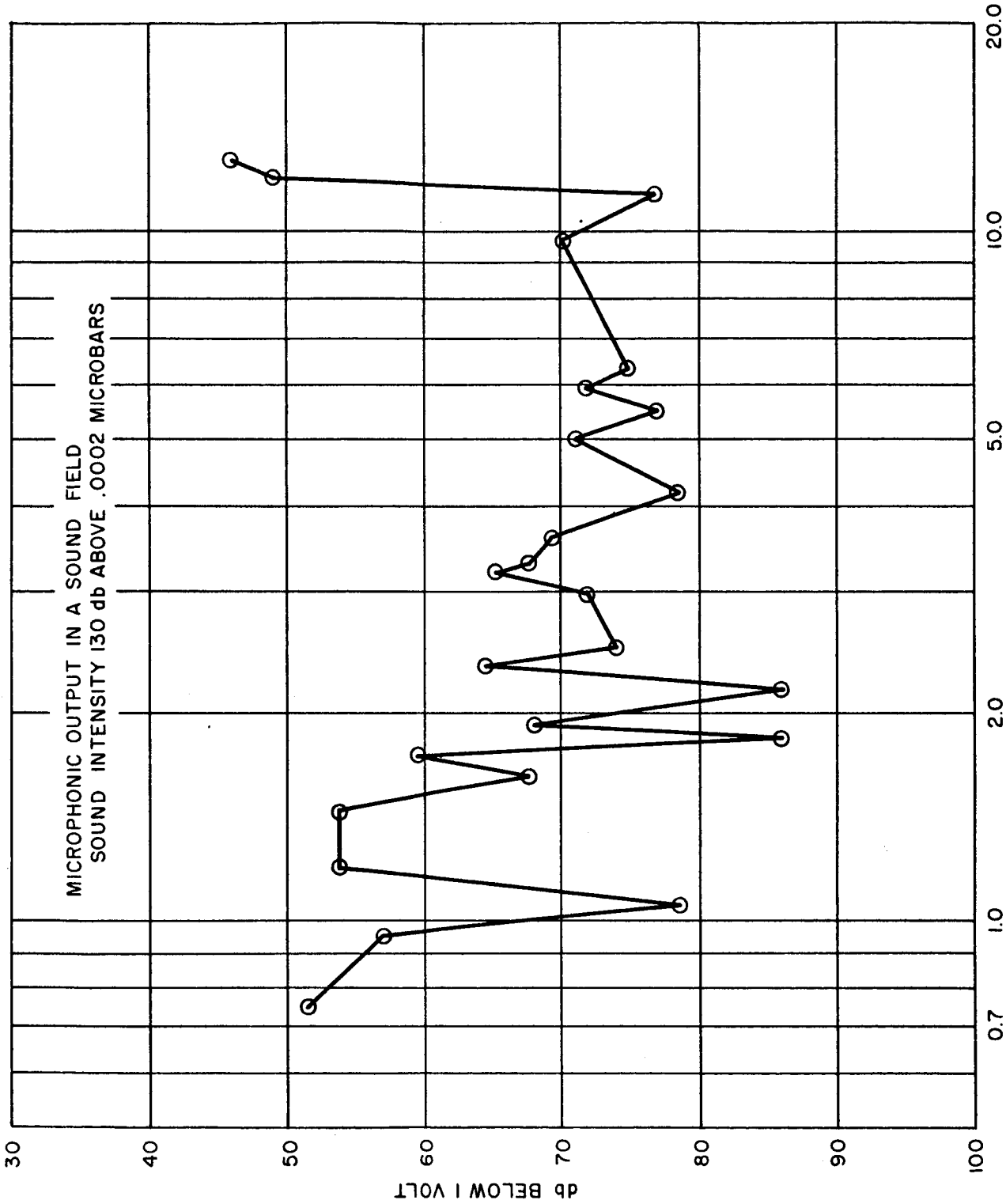


Figure 20. Acoustic Test Results

observed and assuredly genuine peaks between 1200 and 1440 cps, for which the microphonic voltage was 2.2 millivolts.

The packaged delay line was then subjected to vibration and shock, while operating. Vibration in the plane of the ceramic sheet was gradually increased from an initial 2 g's, sweeping frequencies at each acceleration level from zero to 6000 cps. The line withstood all of the vibration tests, to a level of 10 g's. At the last of this run, the feedback accelerometer lost its lead connection, and the table drove momentarily to a power overload. It is estimated that for a few seconds, before power shutoff, the element was subjected to considerably more than 10 g's, and at a frequency well in excess of 6000 cps. Only during this runaway was there an observable level of microphonic output from the line, which was being observed at the reduced level of .050 volts signal output; this microphonic level is estimated to have been about .010 volts.

Shock tests were then carried out, with shock applied at right angles to the ceramic sheet, in the direction of its least strength. Three drops each were carried out at 50 g's, 63 g's, 80 g's, and 90 g's. On the 90 g test a momentary shock wave was observed superimposed on the signal waveform. In all shock tests, an 11 millisecond pad was used.

The resistance to shock and vibration in this mounting is considered somewhat remarkable, since the ceramic sheet and its connecting leads are thin and fragile. It has not been anticipated that a satisfactory mounting could be produced without considerable development. It is believed that the method of packaging and the foam material used are responsible for the success. This particular foam, generically a resilient polyurethane foam, has been measured further to determine its basic properties.

1. Open cell structure. This was originally specified to avoid possible expansion or contraction when subjected to changes in atmospheric pressure.

2. Density 1.8 pounds per cubic foot.

3. Cell size 60 (sixty cells per linear inch).

4. Compressive resilience excellent.

5. Compressive volume - 12:1.

After testing, the delay line package was opened for visual inspection. No damage was found.

4. Delay Line Limitations

The use of ceramic delay lines as a source of power and timing for image converter scanning has definite limitations. Operational problems that exist with the 9 x 9 model indicate that modifications are necessary before larger arrays can be read out accurately. The most important problems are summarized below.

The voltage output available from the delay lines is limited. A 0.5 μ sec drive pulse of 60-80 volts, with rise and fall times of approximately 20 μsec is required to operate the 9 x 9 model. Higher voltage outputs are needed for matrix reverse biasing schemes, and less efficient although more stable coupling schemes. It is difficult, however, to generate higher voltage inputs and to prevent the increased capacitive coupling into the video output circuit.

The coincident voltage selection scheme is itself somewhat limited since a 2:1 ratio between selection and non-selection voltage conditions must be maintained. An appreciable current flows through these elements with the single pulse voltage, V, because of the increased diode capacitance at forward bias even below the "knee" of the conduction curve. Reverse biasing would allow higher pulse voltages to be used with some improvement, but twice the present delay line voltage is needed to eliminate all diode forward conduction in the non-interrogated elements.

Accurate alignment of the pulse peak from each delay line must occur to obtain the 2V peak. If the pulses occur at slightly different times, the charge storage capacitor will not be fully charged and a reduced signal current will flow for that intersection. Operation of the 9 x 9 model has demonstrated that wavefront velocities within one percent of each other are required. Careful control of delay line fabrication should produce lines within this tolerance. However, the pulse wavefront distribution that is observed to some extent in all lines, interferes with accurate alignment and limits the usable length of the line.

The voltage available from a given delay line tap depends upon the power that has been taken from previous taps. This power, unfortunately, varies with the matrix illumination, where an illuminated element consumes the most power. This dependence is minimized by sampling only a small fraction of the acoustic power available at each tap for use in driving the matrix. This implies a larger drive voltage which is undesirable.

A possible solution to the above problems involves the use of diode clipping circuits to produce a constant voltage, regardless of matrix load. The clipped pulses would have flat tops which would minimize previous timing difficulties. If a higher voltage drive pulse is required, however, noise pulses at each tap become more significant.

The rise time of the delay line interrogating pulse, approximately 100 μsec, is somewhat less than can be achieved with transistor circuitry. When a given charge storage capacitor is being recharged, the magnitude of the charging current is inversely proportional to the voltage rise time. Video current magnitudes, therefore, are lower with delay line scanning.

Most of the delay line acoustic reflection noise can be eliminated through proper poling and damping procedures. Capacitive feed through of a differentiated drive pulse into the video output has been difficult to eliminate and is a severe problem in the 9 x 9 model output. Mounting and shielding techniques may be helpful, but more coupling can be anticipated with more compact packaging.

C. ELECTRONIC SCANNING CIRCUITS

1. Microelectronic Drive Circuit

Recent advances in commercially available microelectronic digital circuits make these units ideal for generating stable, uniform scanning pulses for driving an image converter matrix. Combinations of ripple counters, J-K flip-flops--logic gates, ring counters, and shift registers are potentially capable of generating the sequence of pulses produced by multi-tap delay lines. For purposes of this contract, the J-K flip-flop--logic gate method of pulse generation was chosen on the basis of cost, availability,

and performance. The general scheme involves using each flip-flop to drive its successor, in a ripple carry fashion to derive a series of binary counted digital bits (or addresses) and their complements. These binary digits are then used to gate the successive clock pulses, one at a time to successive outputs. The same gates could also be used for random access to the matrix if binary addresses are available, as from a computer, card reader, tape recorder, or remote interrogation signal source. Since these signals were not available for the test model, provision was only made for internally generated binary sequential addresses. Figure 21 illustrates the general interrogation scheme. Future development of monolithic shifting or counting registers may replace this system when random access is not essential.

The horizontal and vertical scan generators have approximately the same logic configuration. Refer to Figure 22 in connection with the following description. The following terminology will be temporarily adopted to be consistent with common matrix terminology. Columns will be driven with the high repetition rate horizontal scanning pulses, and rows will be driven with the vertical scanning pulses. The clock pulse source drives the 8 J-K flip-flops (labeled 358) on the column driver board, (a partial detail of the decoding logic is shown), along with the gates for driving the sync and blanking signals.

The column blanking signal is used to drive the row gate logic board. Thus, the row gate control current is gated only during the column unblanked period to provide a small blanking pedestal on the video output waveform. The only difference in the row gate logic is the inverted logic pulses in the rows with respect to the column logic pulses. This is to accommodate the PNP and NPN drivers respectively. The logic counting is in even powers of Z and is chosen such that operation is near conventional TV rates. Each circuit board counts to $2^8 = 256$ before recycling.

2. Transistor Gates

The matrix is driven by NPN transistors in the columns and PNP transistors in the rows. The transistors are operated in the switching mode

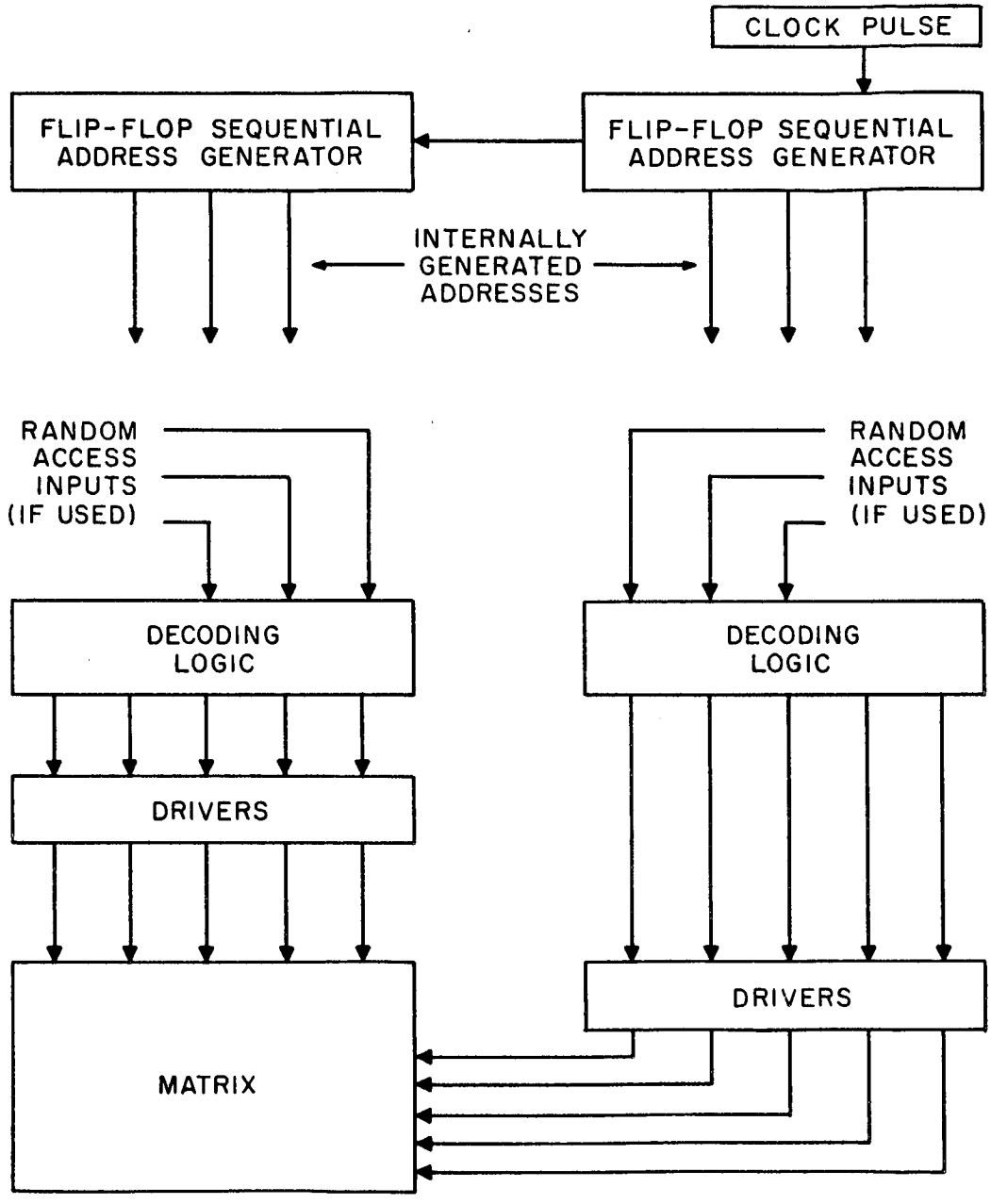


Figure 21. Microelectronic Scan System Diagram

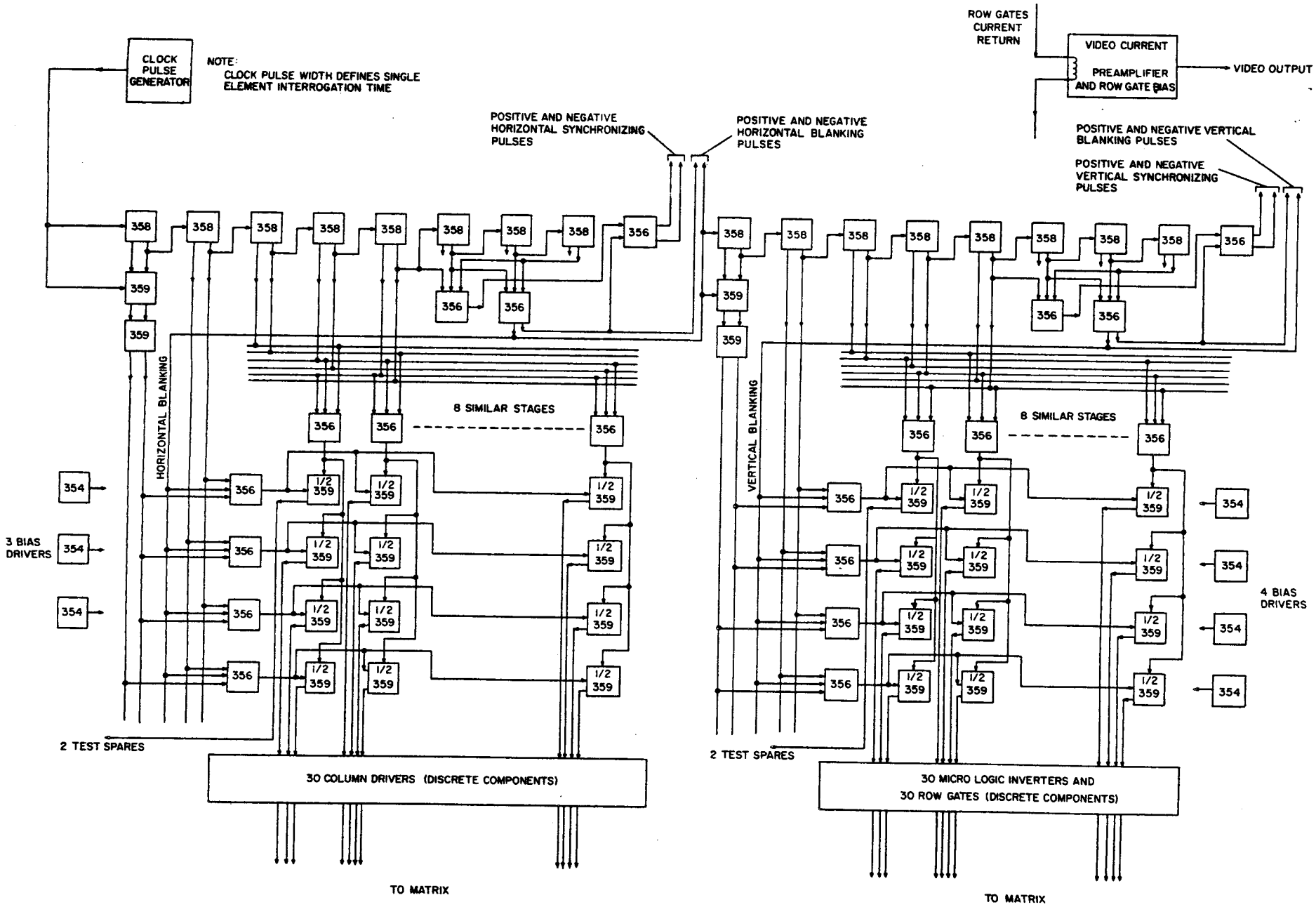


Figure 22. Block Diagram of Micrologic Circuit Scanner

and have very large collector resistances to minimize power dissipation and DC signal current. Hence, any large current which can flow must flow through a matrix storage element. The large resistors aid in reducing cross talk due to a common power supply impedance since they are many orders of magnitude larger than any practical power supplies. Note that the row gates (Figure 23) are driven by DC coupling to eliminate the need for large coupling capacitors. Hence, they have excellent low frequency response. All transistors relax to a nonconducting state when pulses are removed and are active only when pulsed.

3. μE Equivalent Circuit

The operation of the circuit of Figure 23 can be understood more easily by first considering the equivalent drive circuit shown in Figure 24 for a single element. The relative voltages on the row and column lines are those given by the relative voltage diagram of Figure 23. Consider Figure 24 in its relaxed state; i.e., the Row Gate Switch open and the column driver switch open. The matrix element will "see" a bias whose polarity is reverse to its diode and equal in magnitude to $V_R + V_D + V_C$. Closing the row gate switch (column driver relaxed) will apply a reverse bias to the matrix element equal to V_C. Closing the Column Driver switch will apply a reverse bias to the matrix element equal to V_R (with row gate open).

Interrogation of a matrix element corresponds to closing the column driver switch during a time interval in which the row gate is already closed. A transient current will flow through the video current detector charging the matrix capacitor from V_D. Once the capacitor is charged up, the signal current will drop down into the noise level and will be of no consequence. Advantage of this fact is taken in the relaxed fall time of the column driver stage to simplify it, and in the operational model the true fall time constant may be several interrogations long. The amplitude of the charging current pulse is proportional to the degree to which it was discharged by its shunting photoconductor since its previous interrogation. The matrix element operation is detailed in the following section.

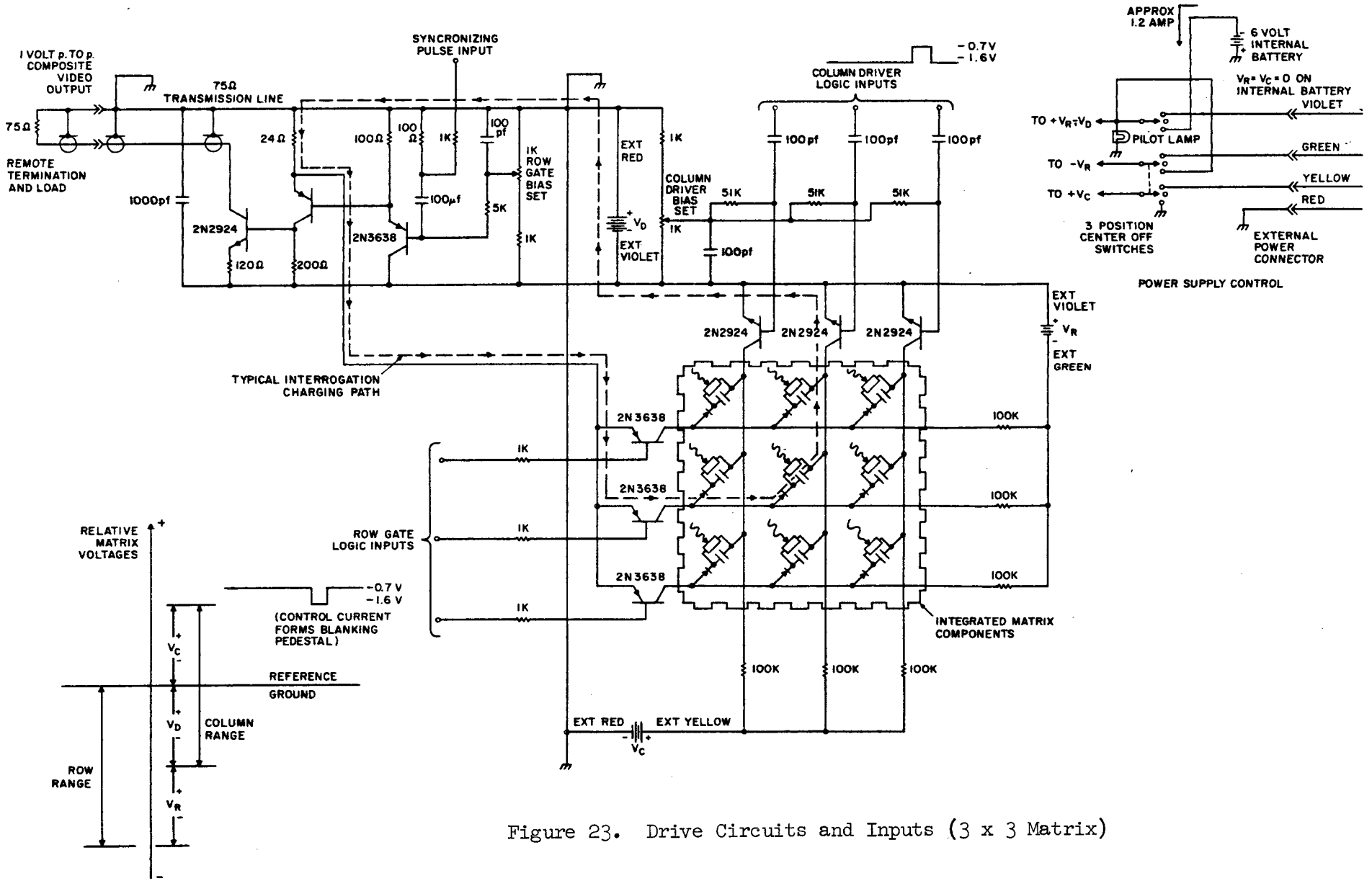


Figure 23. Drive Circuits and Inputs (3 x 3 Matrix)

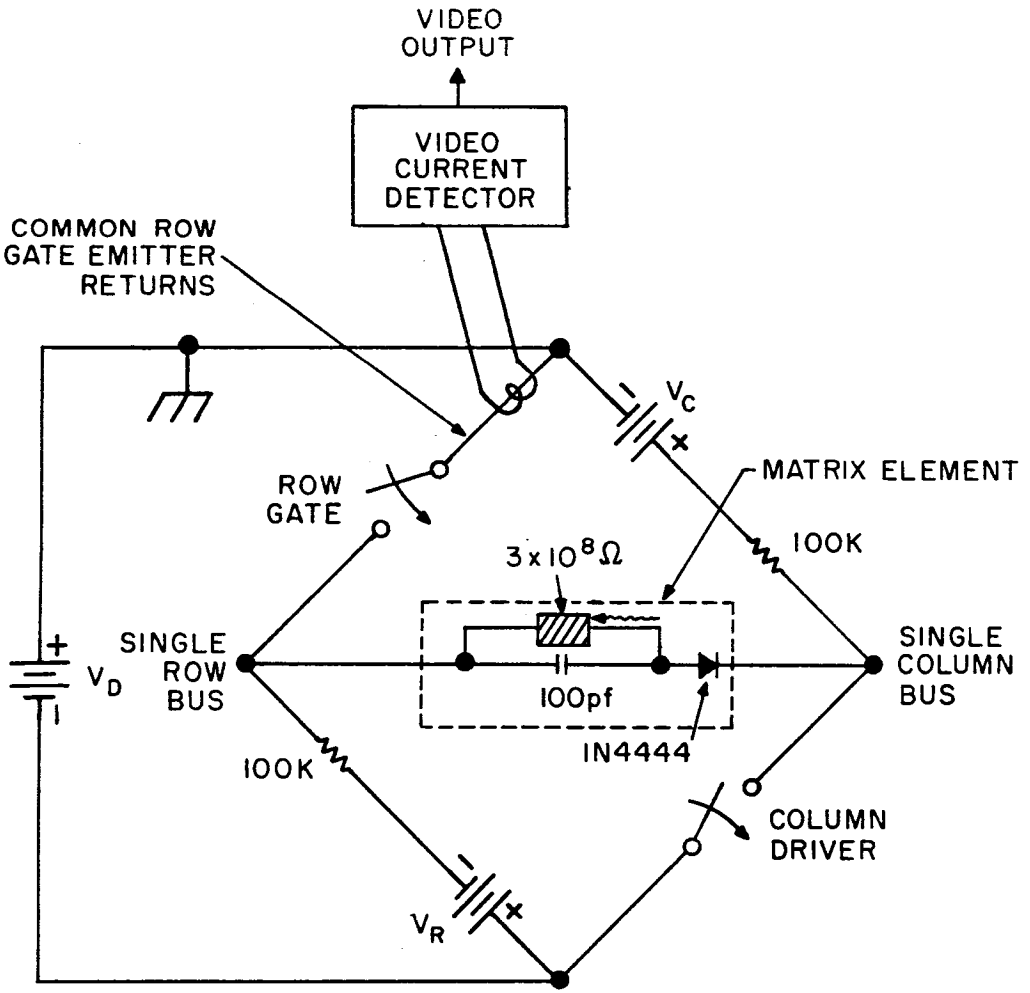


Figure 24. Single Element Equivalent Driving Circuit

Referring back to Figure 23, a typical charging path for a matrix element is traced by the dotted line. The charging path flows through the matrix element, one row gate, one column driver, the output amplifier, and the supply battery. Note that the control current to the row gates also flows through the output amplifier to form the blanking pedestal. External processing would be used to produce a standard blanking pedestal if required. All unpulsed matrix drivers are relaxed to a high impedance state, and hence a negligible current will flow from each one of them. For a large matrix, each of these currents may add up to a small amount and a threshold-type circuit can be used to separate them from the signal. This also is a design constraint on the matrix itself, since the threshold should only be a small fraction of the total signal.

4. Feasibility of Large Array Scanning

Several different approaches to assembling a large set of scanning elements are possible. The major problems are mechanical in nature, and are centered around providing a reasonable fan-in structure of wires from the driver stages to the matrix itself, without introducing an uncontrollable amount of stray coupling paths. The output stages will then be required to be of a custom microelectronic form, either a string of clocked flip-flops each driving the next at the clock pulsed or a decoding matrix and binary address generator. Detailed circuit analysis have not been performed, however, qualitatively less interconnection problems will exist with a string of clocked flip-flops, operating in the desired mode of our output stages. PNP and NPN flip-flop would be required for rows and columns respectively if additional driver stages are to be eliminated. In contrast a matrix of gates would fulfill the requirements also, requiring much less investment in devices, but more in packaging. It is possible to double the number of gates on a single board (compared with the demonstration model) and stack 8 of these boards to achieve a reasonable packing of the required gates for rows or columns using existing techniques. The production of custom microcircuits mounted on a common substrate could produce the required scanning in a fraction of the area used for the demonstration model, and this should be a future goal.

III. IMAGE SENSOR MATRIX

A. MODE OF OPERATION

The image sensor matrix is a two-dimensional array of photosensitive elements that experience a monotonic change in electrical resistance when illuminated. Each photosensor corresponds to one resolvable element of the image focussed upon the array. To form a video signal a known voltage is applied across each two terminal element in turn, and a current flows that is proportional to the illumination.

These elements are interconnected by an x-y matrix of conductors, where one element is located at each conductor intersection. The number of conductors required equals 2N, for an array of N rows and N columns. If individual connections were made to each photosensor, at least N^2 conductors would be required. Figure 25 illustrates such a matrix and the interconnection of each photosensor.

In such a matrix, however, each photosensor has a common connection with N-1 elements of the same row and N-1 elements of the same column and some form of switch must be provided to allow selection of the proper element. In all of the systems investigated and discussed below, a semiconductor diode is used in series with the photosensor with its impedance controlled by the applied voltages of the scanning circuitry. Figure 25 also shows this element.

A number of photosensor configurations have been investigated during this contract. The first to be studied consists of a series photoconductor and semiconductor diode at each matrix intersection. A low resistance photoconductor is required with a resistance range of approximately 10 to 1000 ohms, because of the restricted impedance change available in the diode switch. Such photoconductor elements, however, are difficult to fabricate. The high resistivities of properly prepared CdSe and CdS photoconductor material require element geometries with a high area/conducting length ratio to obtain low resistances. Elements fabricated with interdigital electrodes and utilizing the surface conductivity of polycrystalline photoconductors need a high

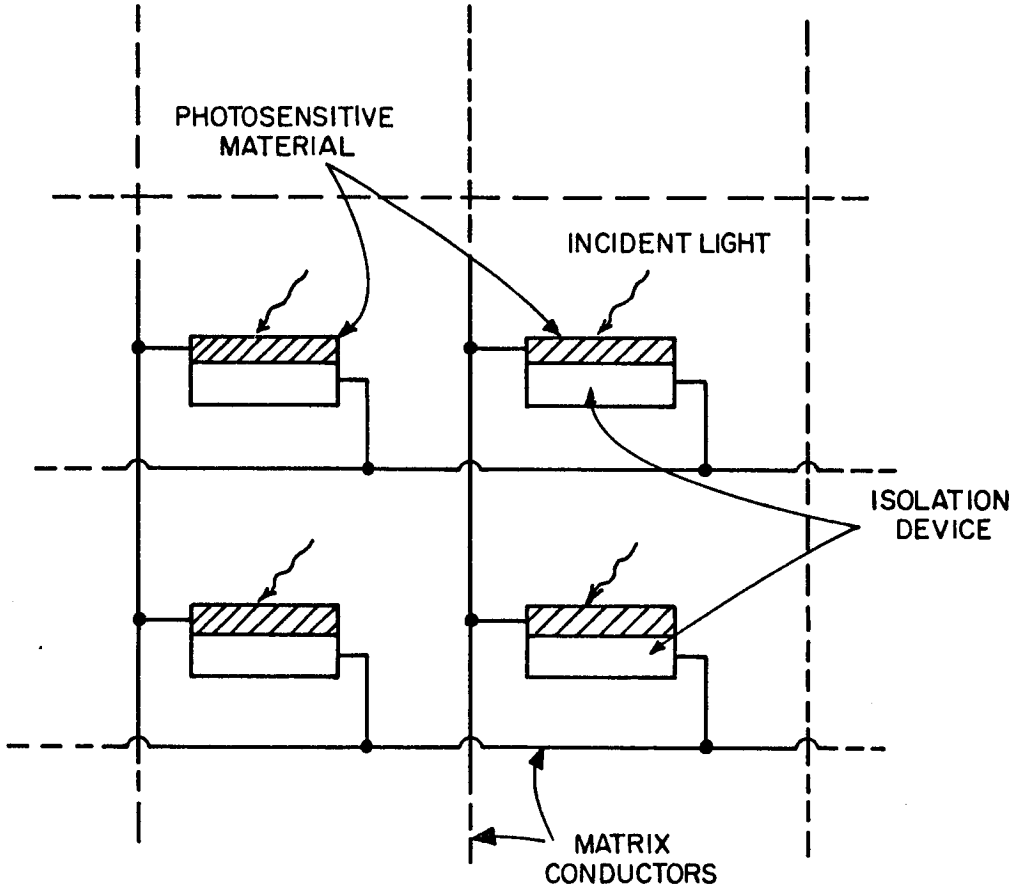


Figure 25. X-Y Matrix Section Block Diagram

folding ratio and consequently, a large area. Elements fabricated in a "sandwich" structure, using transparent electrodes and the bulk conductivity of CdS single crystal photoconductors, were not successful, exhibiting irratic and nonreproducible results. Samples of CdSe were prepared in an attempt to improve the optical time response, but because of the high absorption coefficient, no bulk photoconductivity was observed. Such thin samples of single crystal material are brittle and present a difficult fabrication problem.

The second photosensor configuration studied relieves some of the above difficulties. A parallel combination of photoconductor and capacitor, in series with a semiconductor diode, is placed at each matrix intersection. The capacitor receives a charge from the scanning circuitry and slowly discharges through the photoconductor. The amount of charge that must be added at regular intervals to re-charge the capacitor is a measure of the photoconductor, and therefore the illumination.

The time constant of the photoconductor capacitor combination is of the order of the time between successive interrogations. For conventional television frame rates of 30 per second, capacitor values of the order of 100 pf can be used with high resistance photoconductors of approximately 300 megohms, highlight illumination. These photoconductors occupy less area and are simpler to fabricate than low resistance photoconductors. The reverse bias leakage resistance of the switching diode must be high, to prevent capacitor discharge that is not a function of illumination. This leakage path sets a limit on the low light level sensitivity of the image converter.

In operation, the charge storage made offers an extremely high gain mechanism. The output signal obtained upon interrogation is the ratio of charge to time.

$$i_o = \frac{\Delta Q}{\Delta T_o}$$

The charge on the capacitor is determined by the amount of incident light, which for a photoconductor is directly proportional to the incident photons, times the quantum gain, (G).

$$\Delta Q = G I_i \Delta T_i$$

Thus the transfer function can be written as

$$i_o = G I_i \frac{\Delta T_i}{\Delta A_o}$$

For standard TV rates, $\Delta T_i = 3 \times 10^{-2}$ sec and $\Delta T_o \leq 2 \times 10^{-7}$ sec. The system gain is then 10^5, times the gain of the photoconductor. It is this feature which makes the charge storage mode more feasible than the straight photoconductor detector scheme. This capacitor-photoconductor-diode configuration has been the most successful matrix element to date.

A third photosensor configuration utilizes the light sensitivity of the switching diode, eliminating the photoconductor. The matrix element consists of a series connected charge storing capacitor and light sensitive diode. The diode reverse leakage resistance is a function of illumination and can control the capacitor discharge through the external scanning circuitry. Figure 26 shows the illumination characteristics of an epitaxial diode. The leakage resistance at 10 foot lamberts is approximately two orders of magnitude higher than desired. Reducing the value of the storage capacitance would restore the required time constant, but would also reduce the stored charge and image converter performance. Increasing the diode junction area to reduce resistance degrades performance by increasing diode switch capacitance. A more satisfactory solution is to reduce the frame rate, suggesting that the scheme may be applicable where slow scan readout is employed.

A further photosensor configuration employs a phototransistor in series with a diode switch. Figure 27 shows the illumination characteristics of a single element, interrogated by 0.3 μsec pulses at a frame rate of 30 per second. Output currents are of the order of a few milliamps. Additional tests performed with the microelectronic scanning circuitry and a single element phototransistor diode pair indicate promise for this configuration. The spectral sensitivity of the silicon phototransistor, however, covers a range from 6000 Å to 10,000 Å in the infrared. In addition, a large gain (photons/electrons out) is available from photoconductors, and not available from the phototransistor, although the latter is capable of current gain by a factor of β.

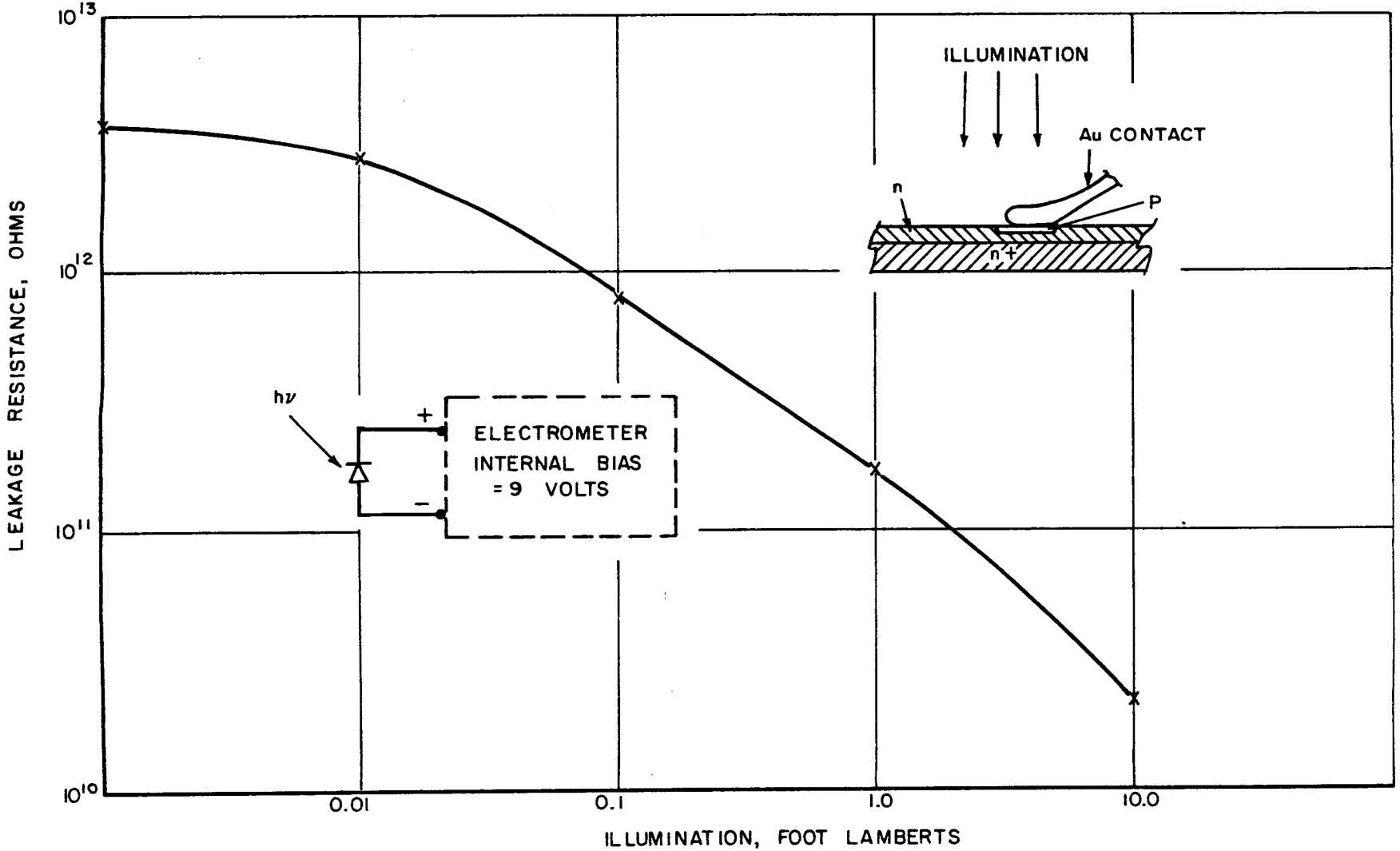


Figure 26. Light Sensitive Diode Characteristic

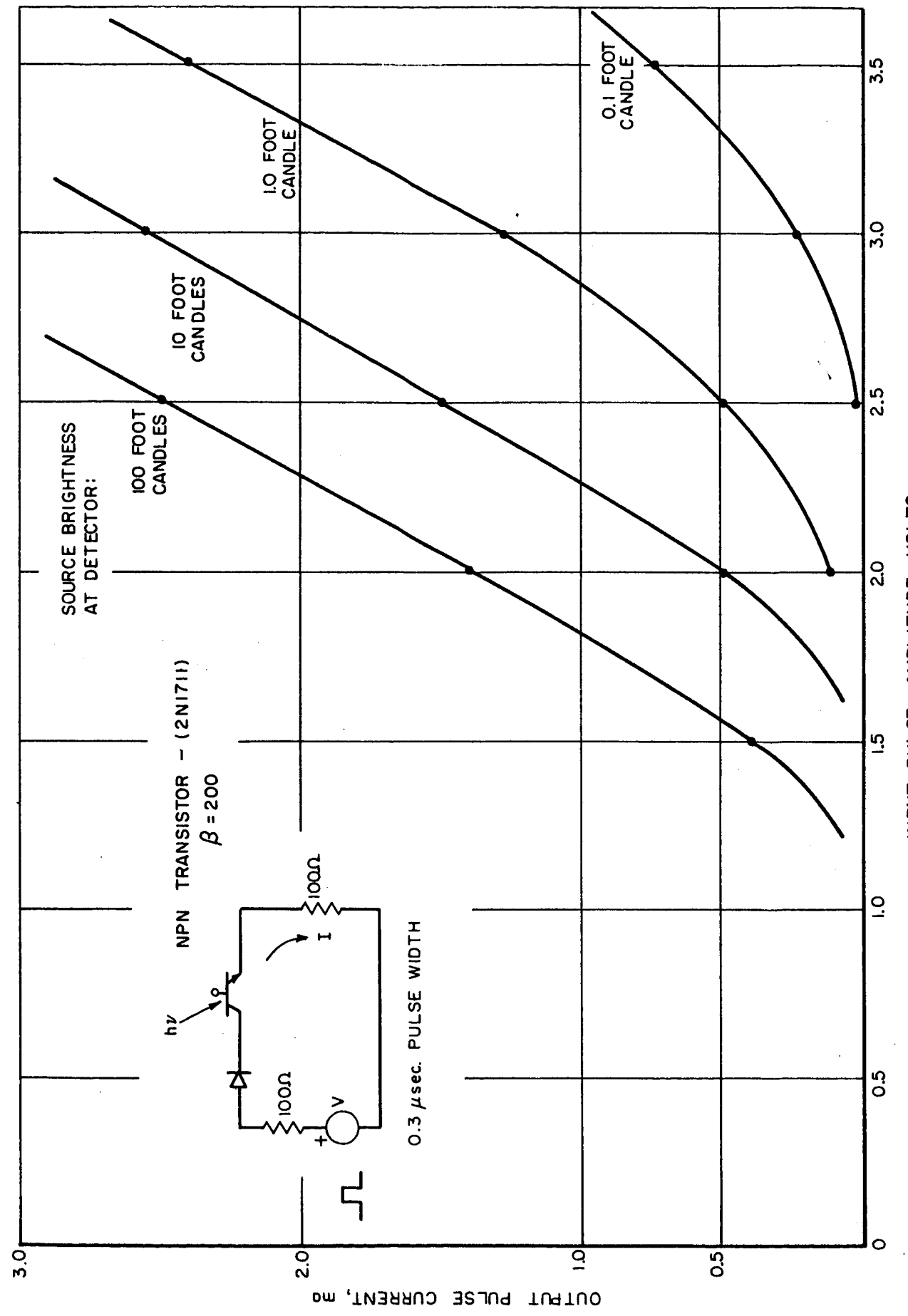


Figure 27. Phototransistor - Diode Characteristics

B. EQUIVALENT CIRCUITS

1. Delay Line System

The schematic diagram of a 16 element matrix with delay line scanning has been shown in Figure 8. The 81 element system whose test results are presented and discussed below is similarly interconnected. Although the matrix conductors are not perpendicular, as in a conventional x-y matrix, each element is in common with (n-1) other elements of the same row and the same column. Each intersection element consists of a semiconductor diode in series with a parallel combination of charge storage capacitor and photoconductor. This schematic diagram can be transformed to the circuit of Figure 28, to study the interrogation of a given element.

In the figure, the conducting path of the outside rectangle contains the signal current. Both activated taps are pulsed simultaneously, overcoming the voltage knee of the three series diodes, and recharging the capacitor of the interrogated matrix element. The charging current flows through the load resistor, from which video output is obtained. The branches inside this rectangle represent the rest of the matrix and the rest of the delay line taps, which are theoretically inactive. The parallel matrix elements consisting of two groups of (n-1) elements, one group of $(n-1)^2$ elements, and two groups of parallel inactive taps. The inactive delay line taps can be grouped into a single element by assuming that the voltage across each tap in the group is equal. All intersection elements are thereby accounted for, since

$$(n-1)^2 + 2\,(n-1) + 1 = n^2$$

Charging currents can flow through these branches and through the load resistor, adding to the video signal. The waveshape of this signal is predictable, but it tends to mask the low level video signals, which then cannot be recovered. In addition, these charging currents disturb the charge storage capacitors, adding or subtracting small amounts of charge from that charge previously stored. Note from Figure 28 that these currents tend to charge the (n-1) element group, and discharge the $(n-1)^2$ group, although

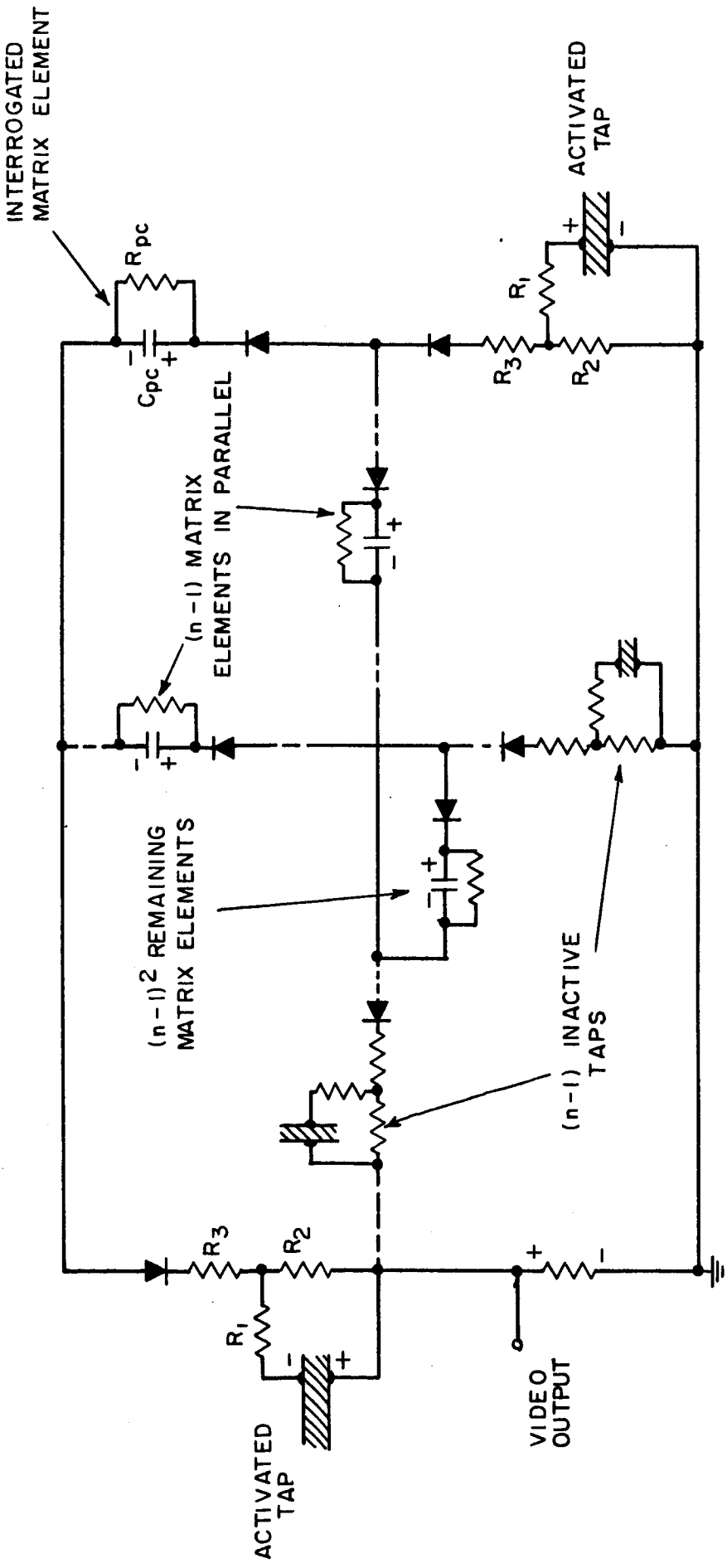


Figure 28. Delay Line Matrix Equivalent Circuit - n^2 Elements

limited in the latter case by the reversed diode. The disturb signals are therefore somewhat self compensating, since each element spends a larger percentage of time in the $(n-1)^2$ group. The additional diodes added in series with the delay line taps are successful in reducing both the video noise and the disturb currents, although requiring more drive voltage. Elimination of these currents is not possible, however, because of the finite capacitance of each diode, and the shunt path that exists within the matrix itself. The effect of this path is discussed in more detail below, with the microelectronic drive system.

As the matrix is made larger by adding more elements, the (n-1) element groups decrease in impedance, and increased noise and disturb currents flow. In a coincident voltage selection scheme where no reverse bias exists to prevent partial switching of shunt branch diodes, the maximum matrix size is severely limited.

2. Microelectronic System

A simplified equivalent circuit of the transistor scanned matrix is given in Figure 29. The form of the circuit is similar to Figure 28, discussed earlier. The outside rectangle is the conduction path for the charging current of the interrogated element. The row driver transistor is shown as a closed switch, and the column driver, as an open switch, about to close. The battery V_b supplies the charging current. The branches inside this rectangle contain the rest of the matrix, and biasing resistors and supplies. The open (inactive) row and column drivers are assumed to be open circuits compared to their bias supplies and are omitted from the diagram. The complete image sensor matrix is shown in outline; it is the same as the delay line matrix of Figure 28, except for the inclusion of interconductor capacitances, C_R (row) and C_L (column). R_R and R_C are the row and column bias resistors. At points labeled b and c, (n-1) of the resistor are grouped to form one resistor of reduced value.

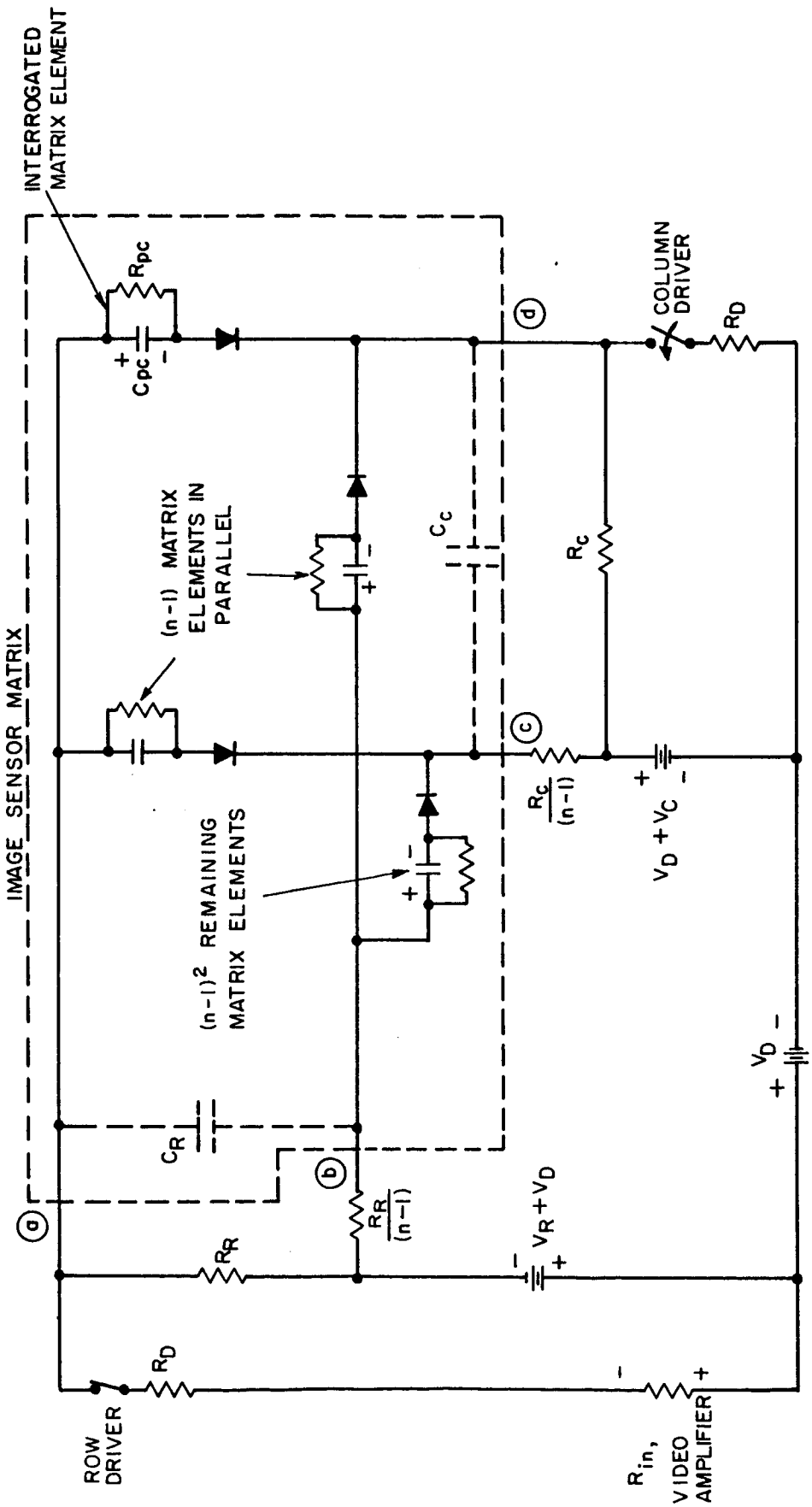


Figure 29. Microelectronic Drive Equivalent Circuit - n^2 Elements

In many aspects, the microelectronic scan differs from the delay line system. The appropriate row driver is always closed for the scan of a particular row, acting as a switch. The column driver only generates the voltage pulse. Precise pulse coincidence is not involved. With the appropriate column driver open, all elements are reverse biased. When the column switch closes, the selected matrix element is recharged with a voltage, Vd, that can be many times greater than the diode "knee" voltage. Noise and disturb current flowing through the other matrix elements are reduced by a sufficient reverse bias that keeps these diodes off at all times. Some of this current can return to ground through the bias source without flowing through R_{in} of the video amplifier. However, a current path exists within the matrix itself, that shunts the interrogated matrix element, and may eventually limit the size of the matrix.

Figure 30 shows another transformation of the equivalent circuit of Figure 29, eliminating the high resistance bias resistors, R_R and R_C, the low capacitances, C_R and C_C and reducing each parallel matrix element group to a single capacitance. The labels, a, b, c, and d in Figures 29 and 30 correspond. This equivalent circuit is valid only for the transient analysis, since all bias resistors are not shown. The capacitances C_1 and C_3 are those of the (n-1) element groups; C_2 refers to the $(n-1)^2$ element group. The resistance, $R_R/n-1$, and $R_C/n-1$ return to ac ground.

A high pass filter of these five components shunts the interrogated element. The capacitance of a matrix element is the series combination of the reverse biased diode and diode stray capacitance Cd, and the charge storage capacitance, C_{pc}. In the 30 x 30 element matrix, C_{pc} = 100 pf and C_d = 2 μf approximately. The total capacitance, therefore, is approximately equal to Cd. The capacitances C_1 and C_3 equal (n-1) (Cd), and C_2 equals $(n-1)^2$ (Cd). For the 30 x 30 matrix and the value of Cd given,

$$C_1 = C_3 = 58 \text{ pf}$$

$$C_2 = 1682 \text{ pf}$$

The series capacitance of C_1, C_2, and C_3 is approximately $C_1/2$ = 29 pf.

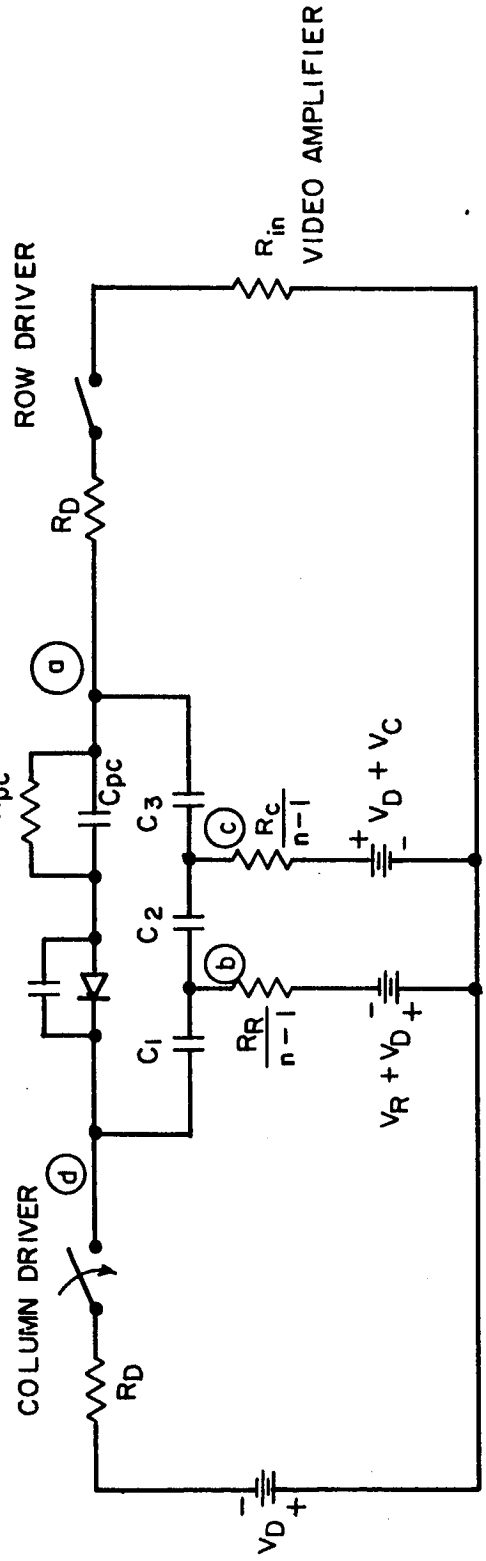


Figure 30. Effect of Matrix Element Shunt Capacity

At interrogation, the selected diode is heavily forward biased and of low impedance. Therefore, the capacitance of 29 pf is directly in parallel with the 100 pf of C_{pc}. Potentially, 22.5% of the video current has flown through this shunt. The actual value can be made somewhat less, depending upon the value of resistors, $R_R/n\text{-}1$, and $R_C/n\text{-}1$, to ground. The bias resistors for the microelectronic driver in use are equal to typically 100K ohms. The shunt resistors for a 30 x 30 matrix are therefore 3.5K ohms approximately. This corresponds to a time constant with C_1 and C_3 of approximately 100 nsec., which indicates little conduction through the resistors to 20 nsec. driving voltages.

These resistances can be reduced to shunt this noise current to ground. However, this will be done at the expense of increasing the disturb currents. The following discussion of the magnitude of the disturb voltages will explain the trade-off available.

When the resistance at nodes b and c are high, the driving voltage from node d to node a divides almost entirely between C_1 and C_3. These voltages further divide according to the ratio of Cd to C_{pc}. The disturb voltage to appear on the charge storage capacitors of C_1 is somewhat less than 0.01 V_D. A large reduction in the value of $R_R/n\text{-}1$ would put C_1 directly across V_D, doubling the disturb voltage.

Note again that C_2 receives the disturb voltage in the reverse direction. That is, C_2 tends to be discharged, where C_1 and C_3 are charged. Although the disturb voltage across C_2 is smaller than the voltages across C_1 and C_3 each element spends a proportionately longer time in the "C_2 group" as the matrix is scanned. The disturb voltages are therefore somewhat self compensating. It appears advisable to use higher values of R_R AND R_C, changing values only to minimize the disturb voltage effect by equalizing the charge and discharge values.

The general expression for the shunting capacitance of C_1, C_2 and C_3 in series is approximately

$$\left(\frac{n\text{-}1}{2}\right) \quad Cd, \text{ for larger n.}$$

The expression for the percentage of total charging current that flows through the shunt is approximately

$$1 + \frac{\frac{2\,C_{pc}}{(n-1)\,Cd}}{100}\ \%$$

To reduce this percentage, and yet increase n, the ratio C_{pc}/Cd must be increased.

IV. DEVICE FABRICATION

A. SUMMARY OF MATERIALS AND DEVICES INVESTIGATIONS

Demonstration of the operating principles of the solid state image detector, as established by the circuit analysis and individual component breadboard models, has been attempted with a deposited structure.

Selecting the charge storage image matrix approach, the following idealized relationships were known:

$$C_{pc} \gg C_d$$

$$R_d(\text{leakage}) > R_{pc}\ (\text{dark})$$

$$R_{series}\ C_{pc} < 0.1\ \mu\text{sec}$$

$$R_{pc}(\text{lit})\ C_{pc} \approx 30\ \text{msec}$$

A predominating influence upon the values selected is the allowable surface area for each of the elements. The resolution selected for this first attempt at an integrated image matrix structure was 50 lines/inch. Thus a total area of 20 x 20 mils could be used for each resolution element. As will be further described in later sections, to achieve isolation between elements, an area of only 16 x 16 mils was utilized for the deposited components.

Although there are many methods of implementing the derived circuit, it was decided that the most favorable approach would be to always select the optimum material to fulfill each particular component requirement. Using this approach, even though introducing additional materials process difficulties, the highest probability of demonstrating the system feasibility would be obtained. It is primarily for this reason then that a silicon diode CdSe PC, and a silicon dioxide capacitor were selected as the final materials.

The circuit that must be fabricated is that indicated in Figure 28, that is a parallel combination of a capacitor and photoconductor, together in series with a diode. Thus, in addition to the three basic components;

interconnections, electrodes, and isolation techniques had to be developed. Development of the needed techniques took place in two steps; first as individual components and second as an array structure.

B. ISOLATION DIODES

The image converter design requires a means of voltage sensing. The device which accomplishes this sensing must have a highly nonlinear current-voltage characteristic with a breakpoint located at a critical threshold value of voltage. In addition, the two-terminal electrical characteristics of this nonlinear switching device must include a low series resistance (on the order of a few ohms) and a low zero-bias capacitance (a few picofarads). Since a silicon diode can have fairly nonlinear current-voltage characteristics and has a breakpoint in the range of 0.4 to 0.6 volt, it was decided to use an array or geometrical matrix of individual diode elements on a common silicon substrate with proper electrical connections as the voltage sensing device. This choice is consistent with the system design philosophy of utilizing the optimum material for each component. While this poses constraints on the fabrication, it assures the highest probability for determining the true potential of the design.

A diode having a capacitance at zero bias of 2 picofarads and a series resistance of 1 ohm would have a theoretical varactor diode cut-off frequency of

$$f_c = \frac{1}{2\pi R_s C_s} = 8 \times 10^{10} \text{ cps}$$

or 80 gigacycles. The design of such a diode for use in a varactor amplifier would indeed be formidable; however, the limits are not as severe in this application. In order to lower the series resistance in the "on" state (bias greater than threshold voltage), conductivity modulation of a thin semi-intrinsic base region of the diode may be used. If the ratio of base thickness, L, to ambipolar diffusion length, L^*, is less than unity, then little voltage drop across the base region will result under high injection conditions. At the same time, the low impurity concentrations of the semi-intrinsic region will form a longer zero-bias depletion region at the junc-

tion and hence reduce the capacitance. As a particular example, for 100 ohm-cm n-type silicon, the donor atom concentration (assuming complete ionization) at room temperature is about 5.2×10^{13} atoms/cm^3.

Assuming degenerate doping on the p-side of the junction with a correspondingly negligible depletion layer, the depletion layer width in the n-type base region is given by

$$t_d = 1.05 \times 10^{-6} \left(\frac{\epsilon(V_o - V_a)}{2\pi e N_d}\right)^{1/2} \quad \text{cm}$$

At zero bias, $V_a = 0$ and V_o is essentially given by the difference between the fermi levels on the two sides of the junction expressed in electron-volts. In this case it is assumed to be approximately 0.6 eV. The zero bias capacitance is then given by

$$C = 1.05 \left(\frac{\epsilon e\, Nd}{8\pi V_o}\right)^{1/2} \quad \mu f/cm^2$$

or for silicon, $C = 2.77\ \mu f/cm^2$.

Then, for a total junction capacitance of 2 pf, the area, A, is given by

$$A = \frac{2 \times 10^{-12}}{2.77 \times 10^{-6}} = 7.23 \times 10^{5}\ cm^2 \quad .$$

This corresponds to a circular area with a diameter of 9.6×10^{-3} cm or 3.77 mils, a reasonable size for diodes to be fabricated in an array. Therefore, the only difficulty lies in maintaining a low series resistance. Since the depletion layer depth is 1.06×10^{-10} cm or 4.17×10^{-8} mil, there is little chance of the depletion layer "punching" through a high resistivity base layer of any finite measureable thickness.

Evaluation of the available devices produced by the G.E. Semiconductor Department indicated that a closely matched device was available in an array form. The SD-300 diode is a 4.2 mil diameter diode on 20 mil center-to-center spacing. The forward characteristics are shown in Figure 31.

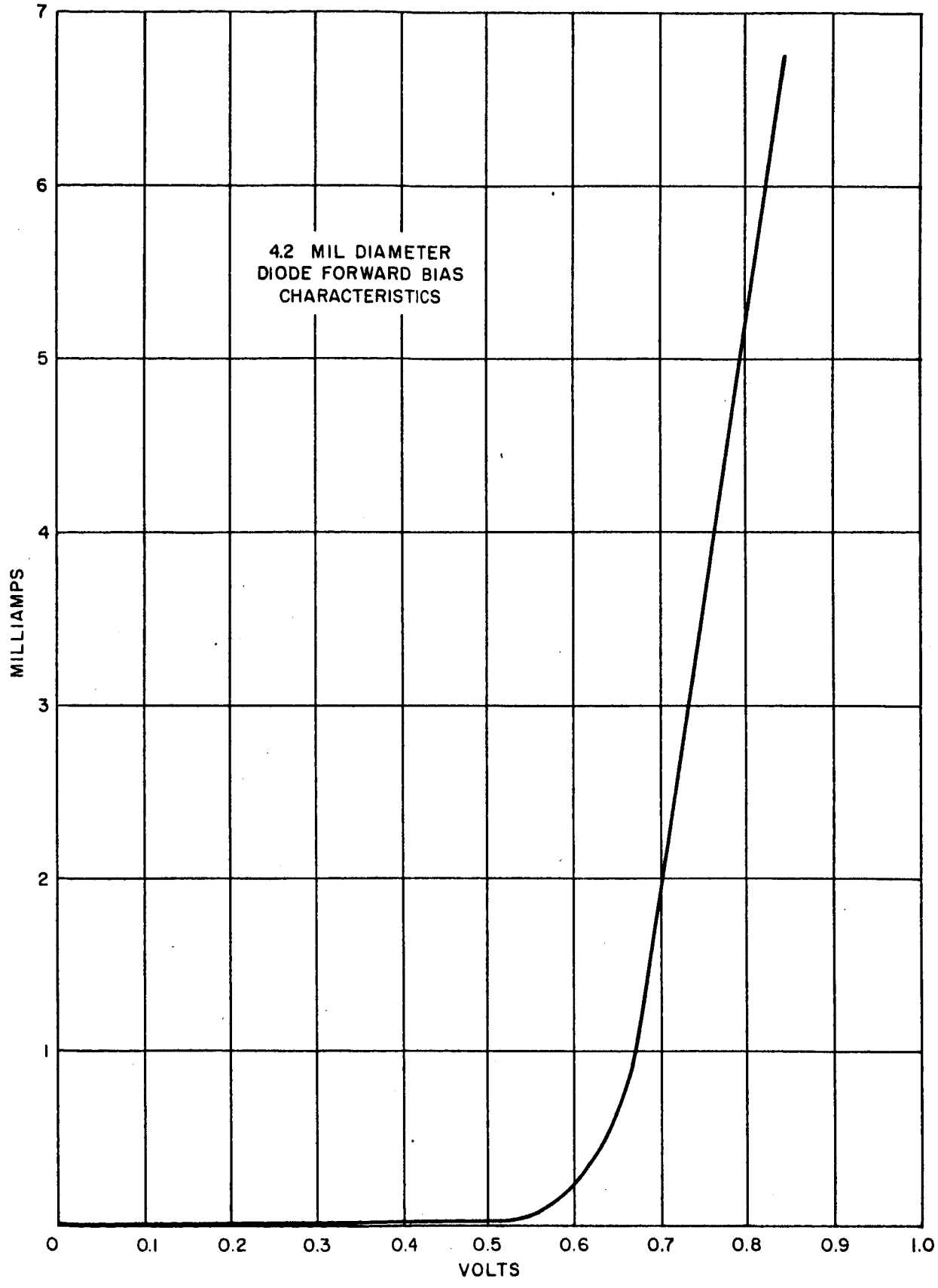


Figure 31

Diode Characteristics

Evaluation of the critical parameters indicate the following results:

$R_{leakage}$: $10^{10} - 10^{11}$ Ω

$C_{zero\ bias}$: 1.5 - 2.5 pf

$R_{forward}$: < 10 Ω

A further requirement on the diode is that is withstand the subsequent processing steps, including sputtering of electrodes and firing at photoconductor processing temperatures.

After sputtering .016" x .016" platinum contacts over the diode dot and firing at 480°C for 30 minutes (the processing temperature for CdSe photoconductors) the leakage resistance was found to be unaffected, or actually increased in some cases.

The capacitance formed between the 16 x 16 mil platinum area and the n-type silicon, the thermal SiO_2 being the dielectric, acts to shunt the diode and increase its capacitance. A total effective junction capacitance of 5.4 pf was measured across a single unit, indicating a parallel capacitance of 3.4 pf in addition to the 2.0 pf junction capacitance. This is one definite limitation to the present device and any future devices of higher resolution would have to minimize this added capacitance. There are two effective methods to do this: increase the thickness of the thermal SiO_2 on the Si wafer, or else reverse the diode wafer and build the structure on the n-type surface where there would not be any effective shunting.

In addition to performing the isolation, the entire diode array is used as the substrate upon which the photoconductor-capacitor films are deposited. A particular advantage to this is that the single crystal silicon can be cleaved on several different planes, thus offering the possibility of isolating rows and columns by mechanically separating the individual elements. This is discussed in a following section.

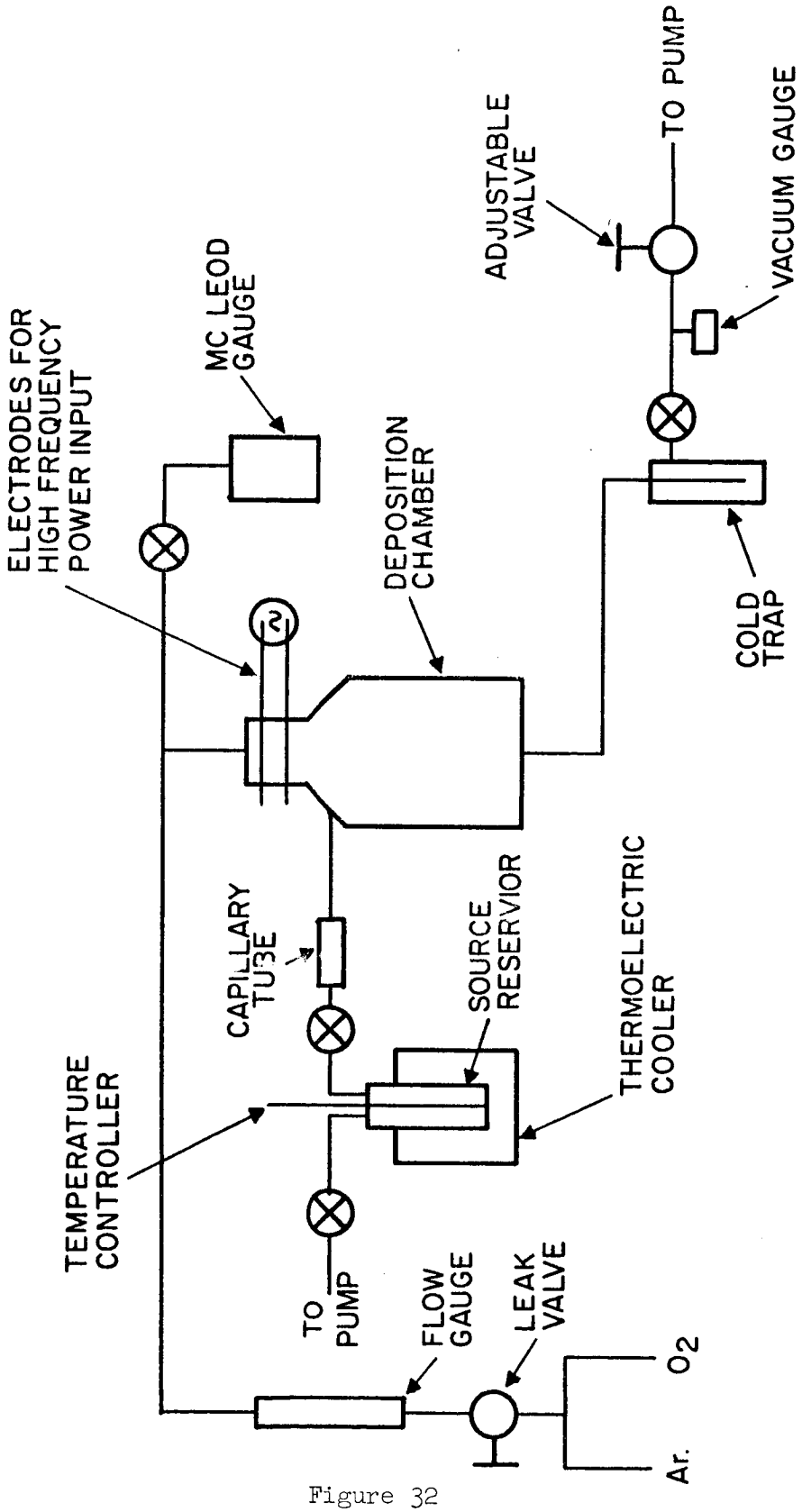


Figure 32

Vapor Reacted SiO_2, System Diagram

C. THE CAPACITOR DIELECTRIC: PLASMA DEPOSITED SiO_2

In order to provide capacitors with low dielectric losses, high values of capacitance with small areas, and stable characteristics, a good thin film dielectric was an absolute necessity. Since the overall microstructure requirement imposed processing temperature limitations and required pin hole free oxides which were not hygroscopic; thermally grown, sputtered, evaporated or thermal pyrolytic processes involving the deposition of SiO and SiO_2 were not satisfactory. Thin film capacitors have been successfully formed by a process[1] which deposits thin pin hole free films of SiO_2 at room temperature by employing glow discharge techniques.

As with thermal pyrolytic processes, an organic source (tetraethoxysilane) is employed, but in this process it is pyrolyzed by an ac induced glow discharge. An r.f. plasma is formed in oxygen which surrounds the substrate. The tetraethoxysilane vapor is then fed into the reaction chamber in the vicinity of the substrate. This vapor is pyrolyzed by the oxygen plasma and SiO_2 is deposited directly on the substrate while the reaction products are continuously pumped out. While only oxygen was used during the course of this project, argon-oxygen can also be employed.

The flow system for this process is shown in Figure 32. The tetraethoxysilane source temperature is cooled via a thermoelectric cooling apparatus so that the source vapor pressure can be held to a controlled level. The oxygen is introduced via a lead valve and its flow rate is continuously monitored with a flow meter. The pressure inside the chamber is monitored with both a McCleod gauge and a thermocouple tube gauge. The cold trap is immersed in liquid nitrogen and collects the condensed volatile by-products of the reaction as well as any unused source so that contamination of the vacuum pump oil is minimized.

The glow discharge reaction chamber is shown in Figure 33. The substrate is supported as a fused quartz pedestal; the pedestal itself is hollow with openings cut in it to allow the various reaction products to be pumped out.

[1] S. W. Ing, Jr. and W. Davern, J. Electrochemical Soc., 112, 284 (1965)

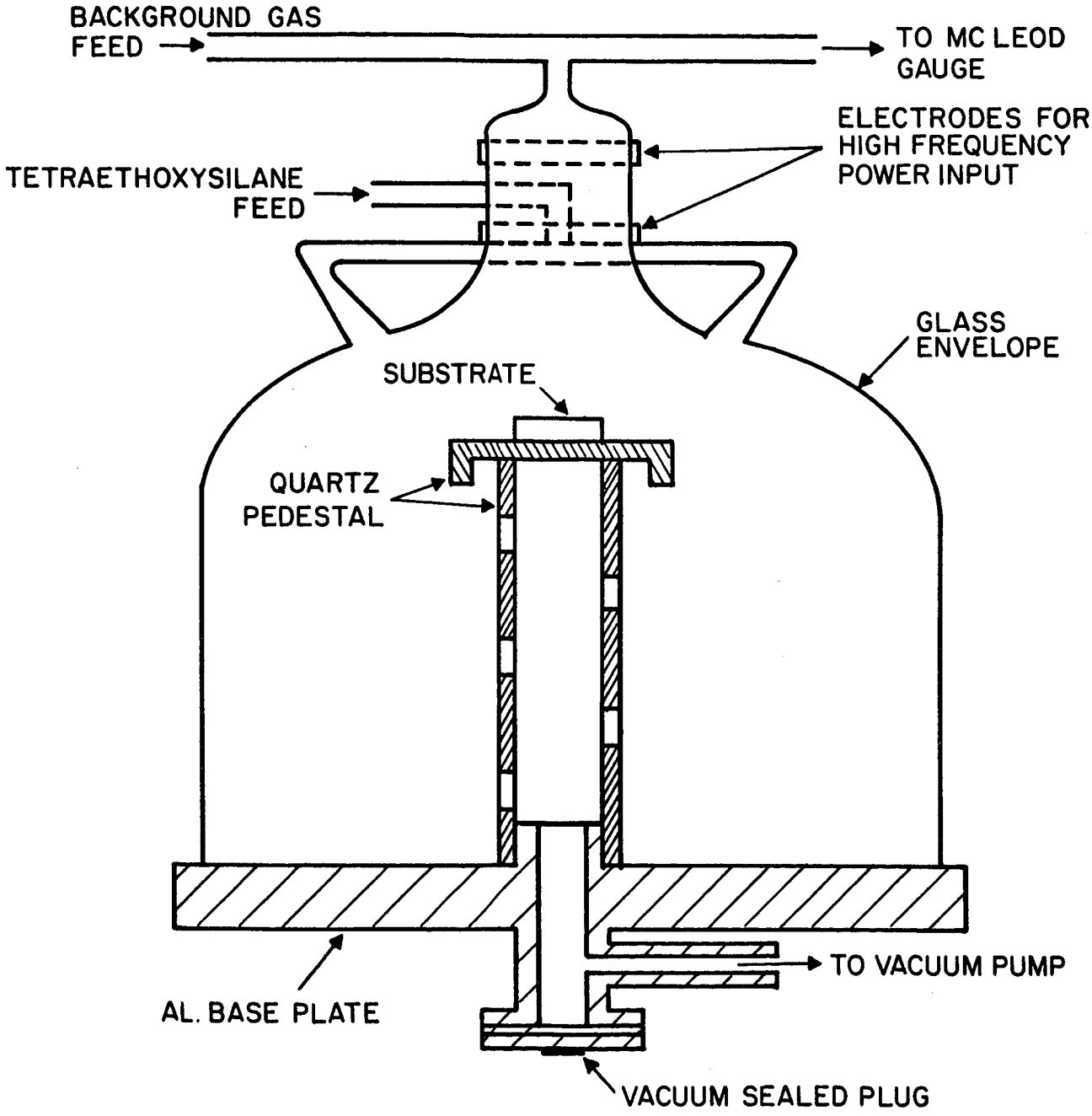


Figure 33

SiO_2 Deposition Chamber

The glow of the ionized plasma occurs mainly between the two electrodes, but extends far enough down into the region where the substrate is located so that bulk of the reaction takes place there.

The oxide films thus formed are amorphous, quite free of pin holes when deposited onto flat smooth substrates, chemically inert, have an index of refraction of 1.5 ± 0.1 (measured with 5460 Å illumination), and have values of dielectric constant lying in the range of 4.5 to 5.5. It has been found[1] that capacitors formed with this dielectric show lower loss tangents when formed with low deposition rates (low source temperature and hence low vapor pressure).

The process as used to form capacitors for the image converter structure involved first the evacuation of the plasma chamber, establishing the equilibrium oxygen pressure between 90 and 100 microns and then prebombarding the substrate with the plasma prior to deposition. When a pressure equilibrium had been reached with the plasma on (at pressures of 100 to 130 microns), the source was turned on. The best capacitors were formed when the thermocouple gauge was kept in the range of 25 to 35 microns (the actual McCleod gauge pressure varied between 150 and 180 microns).

Capacitors formed on glass substrates with previously sputtered platinum bottom electrodes and subsequently evaporated metal film top electrodes were evaluated with respect to both capacitance and leakage. The best capacitors were formed using an SiO_2 film thickness of at least 1500 Å. Capacitors made with 1000 Å SiO_2 film thickness (and sometimes with 1500 Å) showed excessive leakage due to shorting. It is believed that this may, in part, result from irregularities at the edges of the sputtered platinum bottom electrodes which arise from the KPR process used to define the area of these electrodes. This difficulty lead to the choice of 2000 Å for the thickness of the SiO_2 film deposited on the final image converter substrates.

The structure used to evaluate the capacitors utilized sputtered platinum rectangular base electrode on a microsheet glass substrate, with the dimensions of 10 mils by 16 mils. Five such areas on 20 mil centers are on each substrate.

Over this, 1500 Å of SiO_2 was deposited. The top electrodes were formed by evaporating a 1000 Å thick stripe of gold. Both the leakage resistance and capacitance were measured prior to and after a post firing in air at 480°C for 30 minutes. This firing simulated the sintering process needed for the photoconductor to be added at a later part of the image converter processing. The capacitance was measured using a 3 volt rms signal at one megacycle with a Boonton model 75A bridge. The leakage was measured with a 10 volt dc bias and a Bruel and Kjäer model 2423 megohmmeter.

The results are shown below. The capacitances of the four separate electrode areas are quite uniform both before and after firing with a change of approximately 24% between the two sets of measurements. Samples 3 and 4 exhibited lower resistance values after firing; this may be caused by metal migration into the films near the edges where the SiO_2 may have been much thinner than the 1500 Å nominal values as previously discussed.

	Before Firing		After Firing	
Sample	C(pf)	R(ohms)	C(pf)	R(ohms)
1	37	4×10^9	28	10^{10}
2	37	10^{10}	28	10^{10}
3	37	10^{11}	28	5×10^6
4	36	10^{11}	28	2×10^7

If a relative dielectric constant of 4.5 is assumed for the deposited SiO_2, then the calculated value for the 10 x 16 mil capacitor is 27 pf, which agrees well with the cells having undergone post-firing.

D. PHOTOCONDUCTORS

1. Theory and Operation

The photoconductor, as used in the image sensor matrix, provides the important transformation of photons to electrons, allowing the incident light intensity to be measured electrically. In the mode of operation selected, the photoconductor serves to discharge the charge storage capacitor

in proportion to the light received. As shown in section III-A

$$i_o = G \cdot \frac{\Delta T_i}{\Delta T_o} \cdot I_i$$

where G is the gain of the photoconductor in units of electron/photon. From this expression it is apparent that an increased photoconductor gain will increase the sensitivity of the device.

Although most semiconductors and many elements exhibit photoconductivity the gain function is not present in most materials. It is only those materials which exhibit impurity photoconductivity which exhibit gain. Most important among these materials are CdS and CdSe, although other important photoconductive materials having lesser gain are PbS, PbSe, and Tl_2S.

Photon excitation of the photoconductor releases electrons and holes from the valence band and raises them across the energy gap of the particular material used to the conduction band. From the conduction band these free carriers are recombined at capture centers which exist in the host crystal. For most materials the holes are quickly captured and only the electrons contribute to the conductivity of the material.

The recombination centers are of two types; thermal, which lie just below the conduction band, and from which the electron may be thermally released, and ground states which are more remote from the conduction band and from which photon excitation is required for release.

During the lifetime of the free-electron, which includes only the time during which it is in the conduction band, the conductivity of the material is increased. When electrodes are attached to the photoconductor and a potential is applied across these electrodes, the free electrons are accelerated in the direction of the field. If during the lifetime of the free carrier more than one electron can leave the photoconductive material through one electrode, being simultaneously replaced with an electron from the other electrode, the photoconductor is said to possess gain and a current will flow in proportion to the number of optically excited carriers. Gains in the order of 10^3 electrons/photon have been observed in CdSe cells.

2. Materials

The high gain achieved by the recombination center effected lifetime is desirable for the image converter. It is only necessary to provide the proper number and type of defects to create the recombination center. It is a consequence of the achieved gain, however, that the response time is decreased. Thus it is necessary to consider the gain-bandwidth product for the materials, and from the trade-off between of the response time and gain to select a photoconductor.

CdSe and CdS both have G-B products of about 10^5 for low light levels, but the CdSe is nearly an order of magnitude faster, at the sacrifice of gain. Thus even though a more sensitive element could be achieved with CdS cells, the response time would not be well suited to the eventual device. For this reason CdSe was chosen for the program.

Photoconductive CdSe is prepared by properly doping raw CdSe polycrystalline material with copper (acceptor center) and chlorine (donor center). In addition a $CdCl_2$ fluxing agent is used in the sintering process to achieve a uniform doping.

Although the material preparation techniques were developed for sprayed polycrystalline cells, the same doping level of 100 ppm copper and 100 ppm of chlorine was found to give optimum results for the sputtered cells.

3. Electrodes

In general, almost any conductor will provide an electrical contact to a photoconductive layer. If an ohmic contact (linear V-I characteristic) is required, then the work function of the metal must be less than the work function of the semiconductor (for n-type material such as CdSe). This picture is considerably effected by the addition of surface states present in the sintered polycrystalline material. Nevertheless, in order to achieve a near ohmic contact, many commercial photoconductors utilize indium or aluminum electrodes. These electrodes are added, after the firing process, to the top surface of the CdSe. In the circuit structure required to fabricate the image

converter it is necessary to have the electrode on the bottom of the photoconductor, hence deposited prior to firing.

Several metals were investigated to contact the CdSe. The requirements were that the material selected be:

(1) possible to deposit in detailed pattern on the silicon wafer,

(2) make a non-rectifying contact to the CdSe,

(3) be stable under the photoconductor firing process.

Although aluminum and gold fulfill the first two requirements, they would not withstand the atmosphere generated by the 480°C firing of CdSe. Platinum is the only metal that was found to be satisfactory on all three requirements.

The platinum pattern was deposited by a photoresist stripping process. The silicon wafer, (or glass plate in initial studies), was coated with a reverse KPR pattern, i.e., no KPR in areas where the platinum was eventually desired. The platinum was then deposited over the entire plate by either sputtering or evaporation. To increase adherence, a flash of nichrome was first evaporated over the entire surface. This step was introduced when the earlier platinum-only electrodes separated from the silicon in subsequent processing.

To produce the final pattern the entire plate is placed in KPR stripping solution and as the inverse KPR pattern is removed, the platinum on top of the KPR is lifted from the surface. Thus only the desired pattern of platinum remains on the substrate.

This technique was the only satisfactory method found, other than deposition directly through a metal mask, to deposit platinum. The metal mask was not used because of the difficulty of aligning it with the diodes already on the wafer. The standard etching techniques were not suitable because the hot aqua regia used for the platinum attacked the silicon wafer too rapidly.

The one problem seen during the project was the questionable edge shape resulting from the stripping process. In effect the platinum is torn apart and as such makes a potential point of breakthrough for the capacitor to be formed. This is discussed in the section on capacitor dielectrics.

4. Deposition Techniques

A large number of photoconductors have been fabricated during the past several years by a spray and sinter technique. Ratios of light-to-dark current were extremely high for these, ($>10^6$) and the cells were reasonably reproducible. However, the spray process does not lend itself to deposition of the small areas required by the image converter specification. For this reason a vacuum deposited technique was attempted.

Sputtering was selected over evaporation due to the tendency of the individual materials in the photoconductor material to evaporate at different temperatures and thereby greatly change the impurity levels. A diode sputtering apparatus was selected for reasons of its simplicity, ease and speed of operation. It consists of a liquid N_2 trapped pump-station, a pyrex bell jar and a DC power supply. A dual needle valve allows to adjust the (bottle) argon atmosphere in the 8" diameter bell jar to a suitable pressure, maintaining the same current and voltage values within and from run to run. Thermocouple pressure monitoring is performed, but considered of secondary importance since the actual pressure within the plasma is more accurately reproduced by adjusting the argon inlet valve. This, of course, is assuming a constant vacuum thru-put and no mechanical variations of the air passages around the samples, electrode supports and base plate. Innumerable other variables such as electrodes, gas temperature, and vapor pressure of materials to be sputtered were assumed to be about equal from run to run, since sputtering times and materials were essentially the same. In an actual sputtering run the current density on the CdSe over-coated aluminum cathode is maintained at 0.3 ma per cm^2 in order to keep the cathode temperature rise low. The applied voltage of 1.5 kv was selected at a point for which the aluminum cathode would not deposit onto a substrate and yet the CdSe would readily sputter.

A typical deposition consists of cleaning the general glassware within the bell jar and after oven drying, a pump down of the system to assure dryness. An etched aluminum cathode with a sprayed photoconductive CdSe layer is then inserted into the cathode holder. The holder serves as the lead in contact for the negative potential from the regulated DC power supply.

A large number of experiments were performed using the doping levels of the CdSe target as the variable parameter, with the outcome of these tests the selection of the standard doping levels used in sprayed photoconductors. Additional discussion of this parameter is contained in the following section.

The substrate to be coated is placed on an insulated pedestal between the aluminum base plate and the cathode. Since this distance is of importance in respect to the rate of deposition, and other effects, care has been taken in maintaining this parameter. The system is flushed with argon and after reaching a vacuum level of about 1μ, argon is leaked in to achieve the sputtering atmosphere. The actual sputtering is initiated by applying the voltage to the electrodes. A slight adjustment of the argon leak valve must be made after a few minutes of sputtering since adsorbed gas layers on the glass surfaces are, in time, removed by the plasma. A steady current is generally obtained after 3 minutes and is maintained for a total of 30 minutes. Ten minutes of cooling are allowed before removal of the sample. A total of 120 testing samples have been made, one sample at a time. The rate of deposition has been between 8 to 9 angstroms per second for essentially all of the samples.

5. Development of Sputtered CdSe Photoconductor

During the CdSe development a standard test cell was used. This consisted of a coplanar platinum electrode on a glass substrate. Six individual cells, each having a folding ratio (length of gap/width of gap) of 200, were deposited.

Throughout the study, the results were compared with the average sprayed array, since these were considered to exceed the requirements for the project.

	Cell No.	I_L(μa)	I_D(μa)
Plate S_1	1	1200	< .001
	2	1200	< .001
(S for sprayed)	3	800	< .001
	4	740	< .001
	5	1100	< .001
	6	1.200	< .001

Illumination level: 1 Ft.-candle

Bias : 30 VDC

The initial sputtered CdSe photoconductor was made from the identical doping levels and performed as follows.

	Circuit No.	I_L μa	I_D μa
Plate No. 1	1	.8	.058
	2	.006	.0038
	3	1.00	.26
	4	1	.16
	5	.06	.01
	6	.5	.05

Sputtering parameters were:

E = 1.5 kv, I = 6 ma, Time: 1 hr. P ≈ 30 μ

Cathode to target distance 37 mm

Post firing 15 minutes at 400°C in N_2 + 1% O_2

Variations of several parameters connected with the sputtering mechanism such as current density, voltage, pressure and so on, produced only minor improvements. For a considerable number of experiments an average light-to-dark ratio of 20 became almost a standard value. Generally, the obtained light currents were much too low and showed excessive variations over the 6 test cells on one plate. Dark currents ranged too high and were distributed in a similar fashion.

Emission spectroscopic techniques were initiated at this point. They were chosen for the employed doping levels of 100 ppm which are well within the range of this method. The suspected change in stoichiometry ratios was confirmed. Additionally, there was a complete lack of copper in the indicated readings. This reading was compared with a sprayed cell which indicated a strong copper content.

Tracing the process history of the material established that the sputtering cycle introduced the most serious modifications of the CdSe:Cu ratios. Approaching this problem by an empirical method established that at a cathode to target distance of 7.5 mm all materials were present in the sputtered sample, as indicated by emission spectro-analysis. However, a typical test plate measured for photoconductivity showed no improvement.

Plate 11	Circuit No.	I_L	I_D
	1	1.0	.38
	2	2.0	1
	3	1.0	.52
	4	3.4	2.2
	5	no contact	
	6	no contact	

As can be seen by comparison with plate No.1, the previously mentioned gain of 20 had dropped to an insignificant value.

An increase of cathode-target distance to 18 mm showed a slight improvement of $I_{L/D}$ ratios.

Plate 13	Circuit No.	I_L μa	I_D μa
	1	.48	.04
	2	.94	.05
	3	.72	.06
	4	.52	.03
	5	no contact	
	6	.66	.04

The observed drop in light current suggested a needed change of copper doping levels.

A new series of samples were made from starting material containing 25 times the Cu impurities, again varying the cathode to target distance.

Test Plate No. 14 (at 7.5 mm distance)	Circuit No.	I_L μa	I_D μa
	1	.007	.0024
	2	.012	.0022
	3	.018	.0018
	4	.012	.0022
	5	.22	.0018
	6	.018	.0016
Test Plate No. 17 (at 22 mm distance)	1	.003	.001
	2	.14	.005
	3	.08	.003
	4	no contact	
	5	.20	.0064
	6	.18	.006

From this series of tests it was assumed that the important factor was to transport a certain amount of copper. Since this could be effected either by distance or concentration, the control of distance with the copper concentration held at 100 ppm was chosen.

The one key process step that had not been studied was the firing process. Up to this time the plates were fired in an atmosphere and furnace similar to that used for the sprayed sample. Fixing the material and sputtering conditions, a series of tests were made.

Plate No. 19 was post fired at 400°C for 18 hours.

Plate No. 19	Circuit No.	$I_{L\ \mu a}$	$I_{D\ \mu a}$
	1	.10	.001
	2	.14	.001
	3	.015	.0012
	4	.50	.001
	5	.82	.001
	6	.28	.001

After many subsequent test runs it was established that similar results could be obtained by an increase of firing temperature and shortening of firing time. However, the individual tests showed large variations and generally low light currents.

During this phase of the photoconductor-investigation leading up to test plate no. 71, x-ray Lane and diffraction recordings were employed. Optical transmission measurements were made on many nonelectroded test plates for correlation of optical and electrical properties of the sputtered layers of CdSe. It was found that sputtering deposits the CdSe material with a high degree at hexagonal symmetry. An unfired CdSe layer shows, under x-ray diffraction, a single peak at 32° (for a Fe target) or 25.2° (for Cu) corresponding to 0002 planes. Laue patterns reveal a corresponding single d value ring structure. One must, therefore, visualize a polycrystalline layer where the C-axis is aligned in the direction of growth but is other-

wise irregularly oriented. Similar measuring methods applied to a CdSe photoconductor made by a spraying technique show a multitude of crystal planes as evidenced by diffraction and Laue patterns.

These results are shown in Figure 34 for the sprayed photoconductor and Figure 35 for the sputtered photoconductor. Emphasis was, therefore, placed on obtaining firing conditions which would result in structures similar to those observed on sprayed materials. This was done fully realizing that sprayed materials exhibit such highly irregular patterns even before firing and still need to be fired in order to become good photoconductors.

Modification of the firing conditions indicated that a wide range in crystal orientation could be accomplished, and in addition that this was a relative measure of the photoconductivity. Figure 36 shows the results of a good cell. This compares favorably with that for the sprayed CdSe. This photoconductor was produced under the following conditions:

$CdSe + CdCl_2$ + 100 ppm Cr + 100 ppm Cl
E = 1.5 kV, I = 6 ma Time: 1/2 hr. P ≈ 75 μ
Cathode to target distance 18 mm
Post firing 30 minutes at 450°C in air
Post washed in DI water and post rinsed in methanol

Sample No. 65	Circuit No.	I_L μa	I_D μa
	1	5	.008
	2	20	.014
	3	7.6	.002
	4	10	.001
	5	100	.005
	6	30	.012

These encouraging results were improved by the addition of a layer of $CdCl_2$ onto the test plate prior to sputtering, and are shown under testing of plate No. 73.

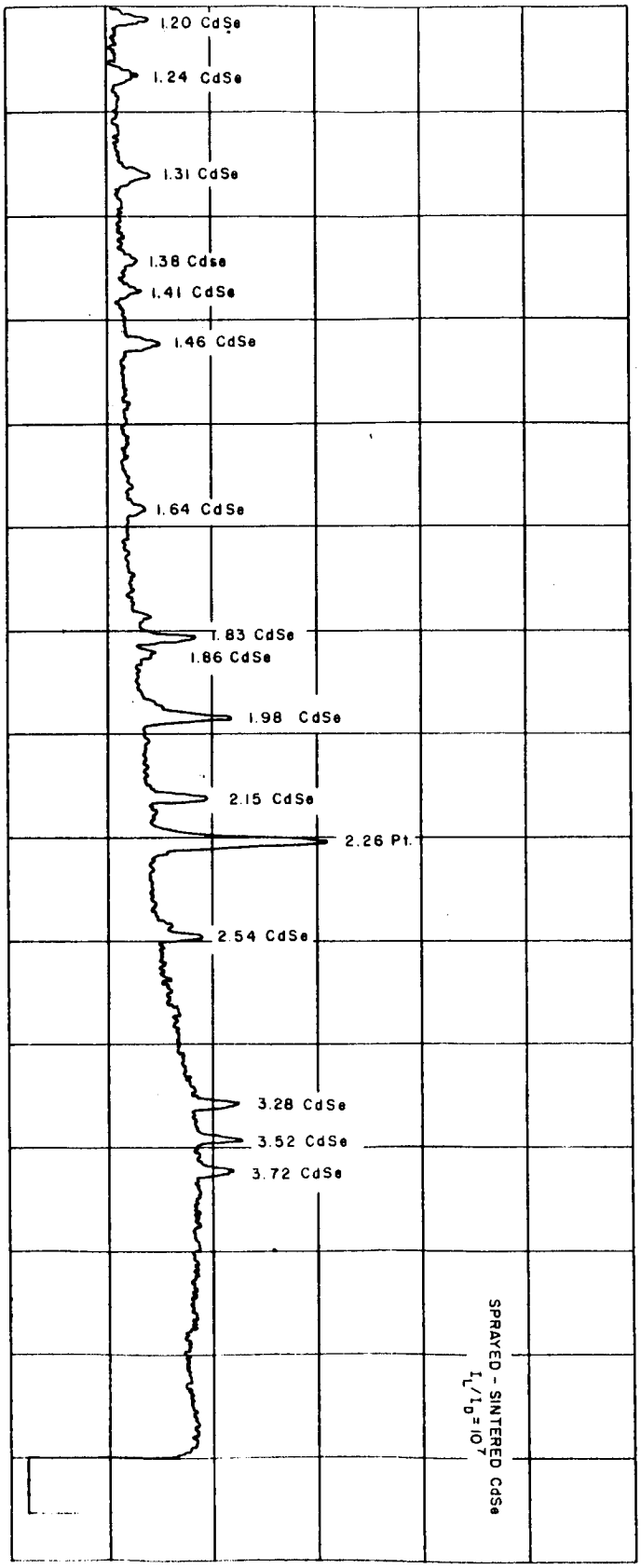


Figure 34

X-Ray Diffraction Analysis-Sprayed CdSe

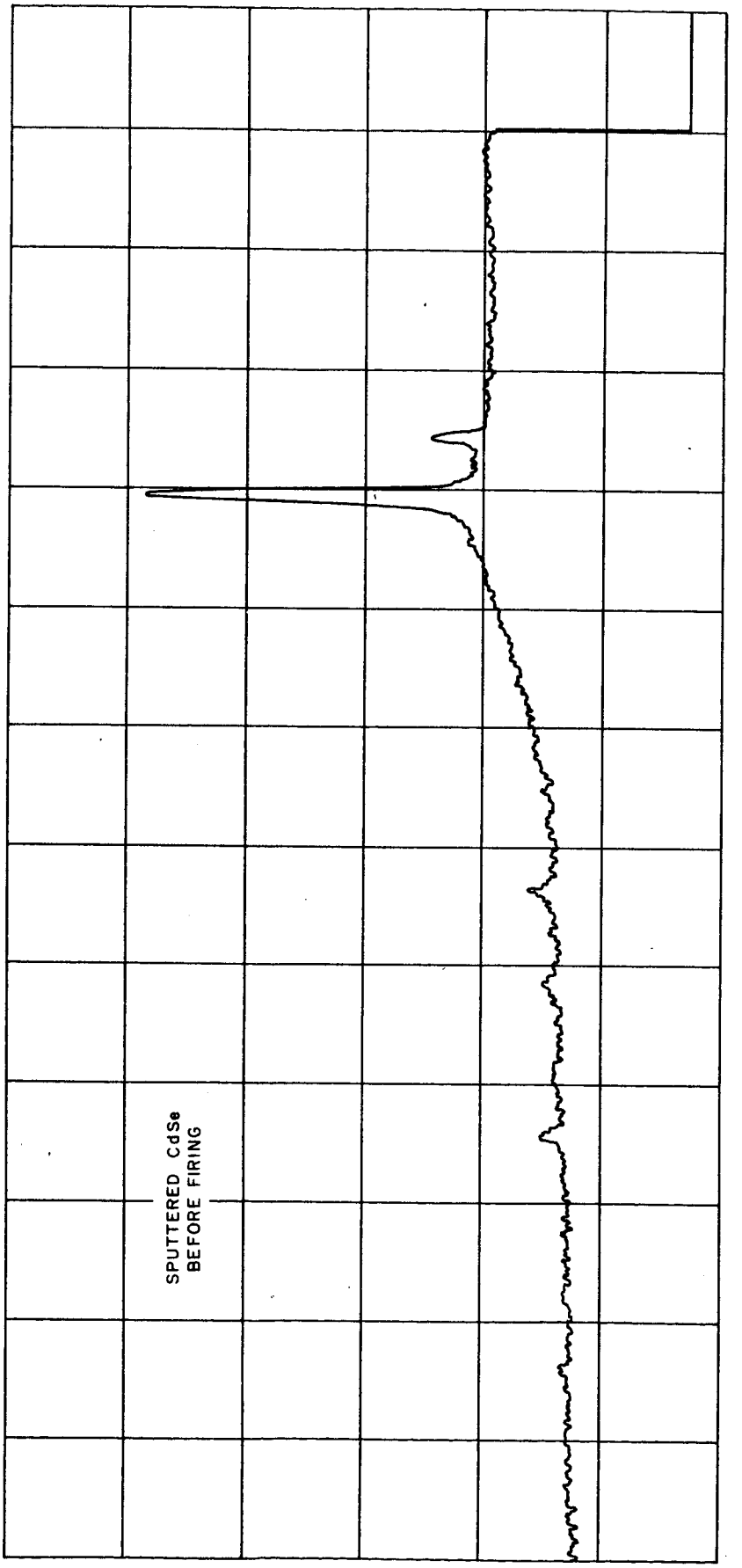


Figure 35

X-Ray Diffraction Analysis-Sputtered CdSe

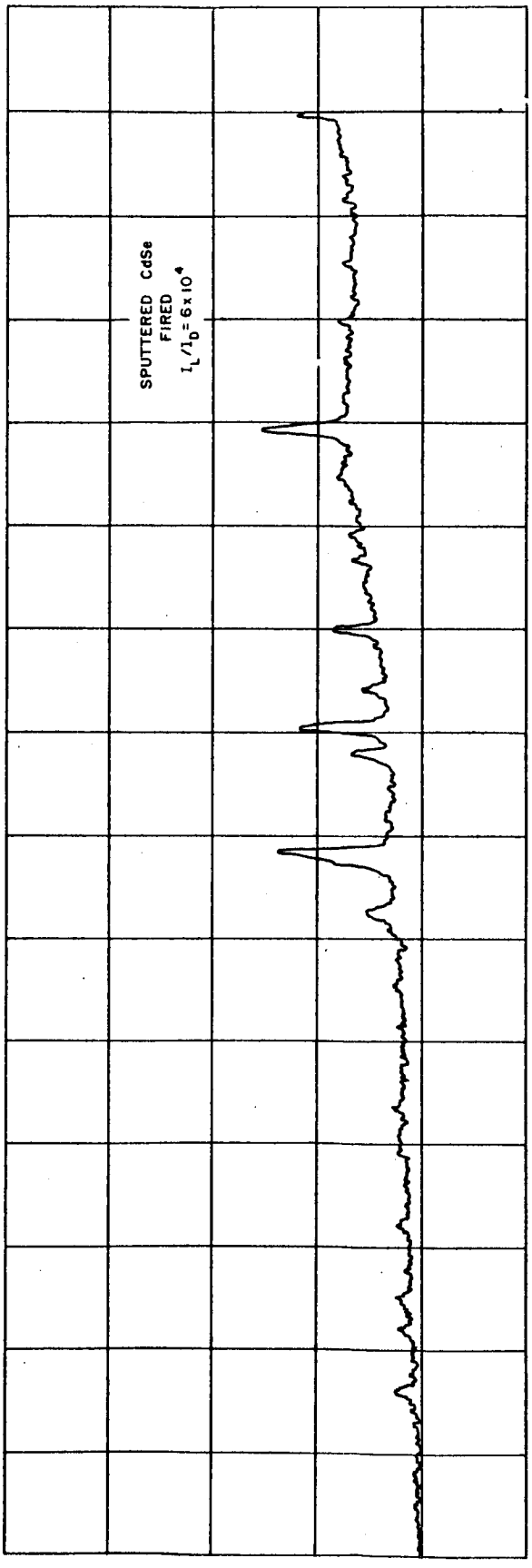


Figure 36

X-Ray Diffraction Analysis-Sputtered and Fired CdSe

Sample No. 73	Circuit No.	I_L μa	I_D μa
	1	5.2	.001
	2	4.2	.001
	3	3.2	.001
	4	2.4	.001
	5	2.0	.001
	6	1.8	.001

Changing the total amount of $CdCl_2$ increased the light current to levels exceeding the required sensitivity of the photoconductor needed for this project.

Sample No. 94	Circuit No.	I_L μa	I_D μa
	1	17	.002
	2	10	.004
	3	12	.003
	4	12	.001
	5	60	.002
	6	100	.001

These results represent an increase of up to 10^5 times of the performance of sputtered CdSe photoconductors at the beginning of this contract.

A number of electrical and optical tests were made on the good cells in order to compare them with the sprayed material, and to help understand the mode of operation.

Figure 37 is a transmission spectra of the sputtered CdSe. The shift in the absorption edge with firing has not been explained.

Figures 38 and 39 indicate the wavelength response characteristic for a sprayed CdSe cell and a sputtered CdSe cell respectively. The sharp cut-off in the near IR region can be attributed to the transparency of the sputtered PC to this light. The wavelength cut-off of about 7200 Å on Figure 37 corresponds closely to the drop in electrical response. The broad band response exhibited by the sprayed cell is attributed to scattering in the rather thick, porous CdSe layer.

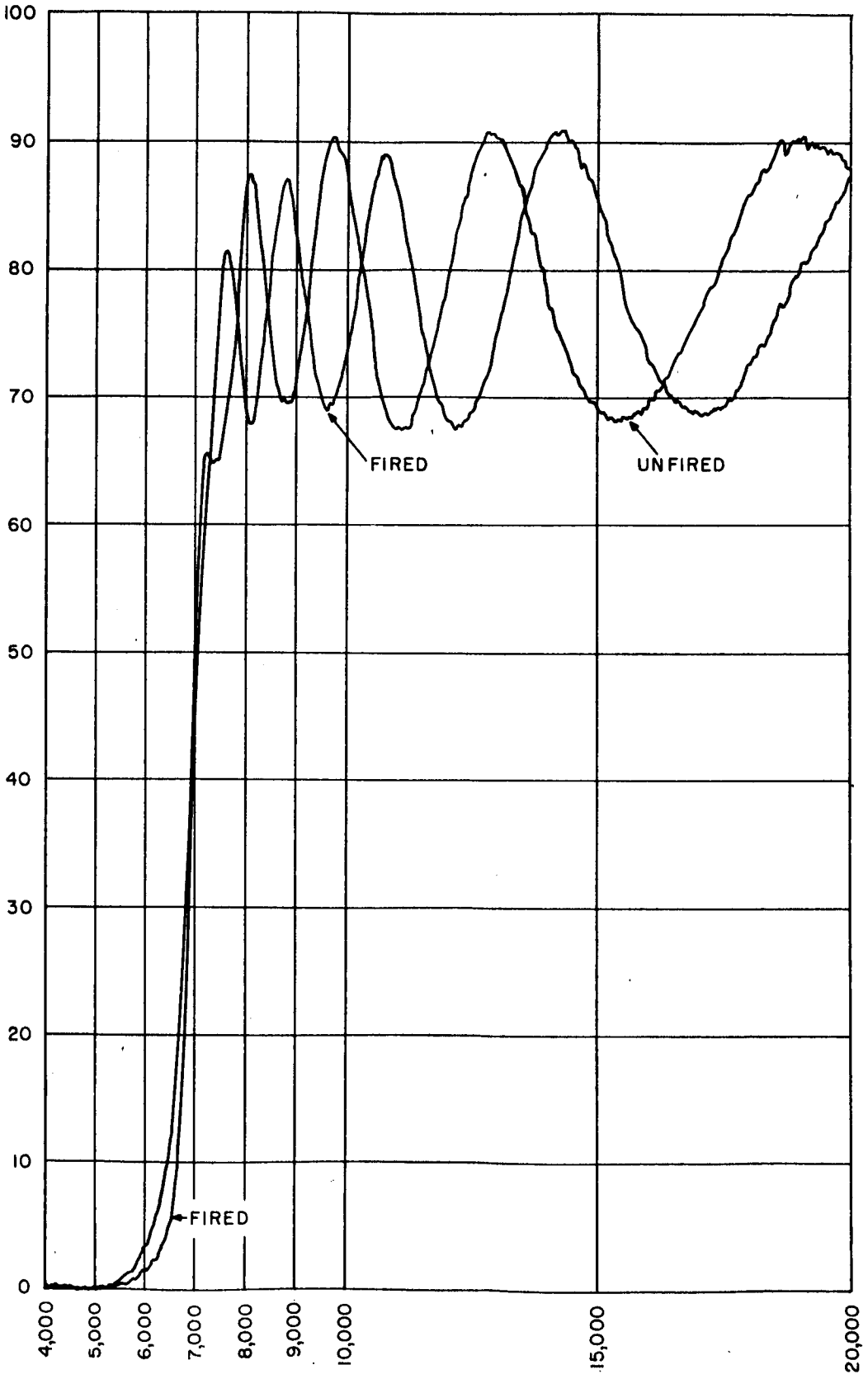


Figure 37

Sputtered CdSe Transmission Spectra

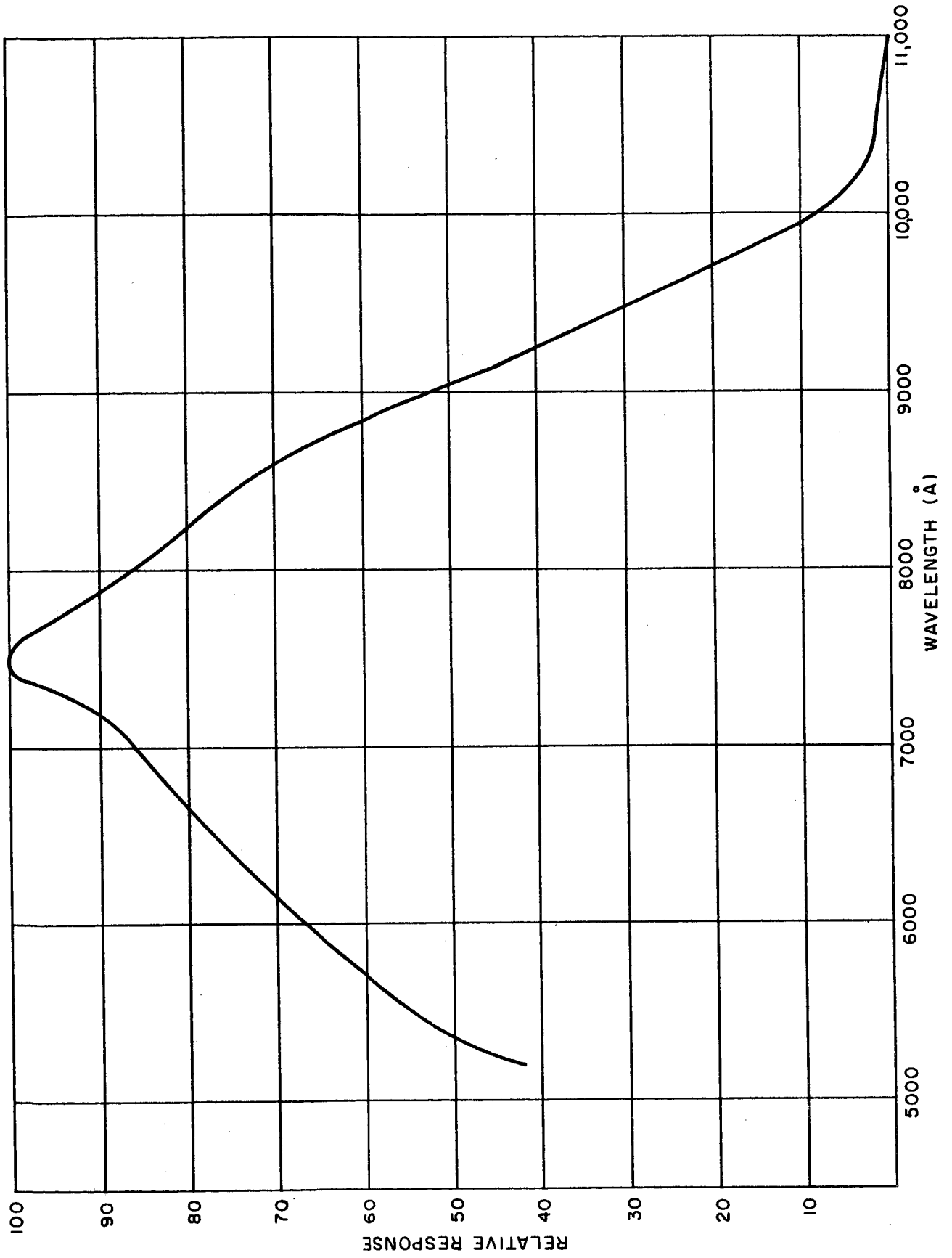


Figure 38

Spectral Response of Sprayed CdSe Photoconductor

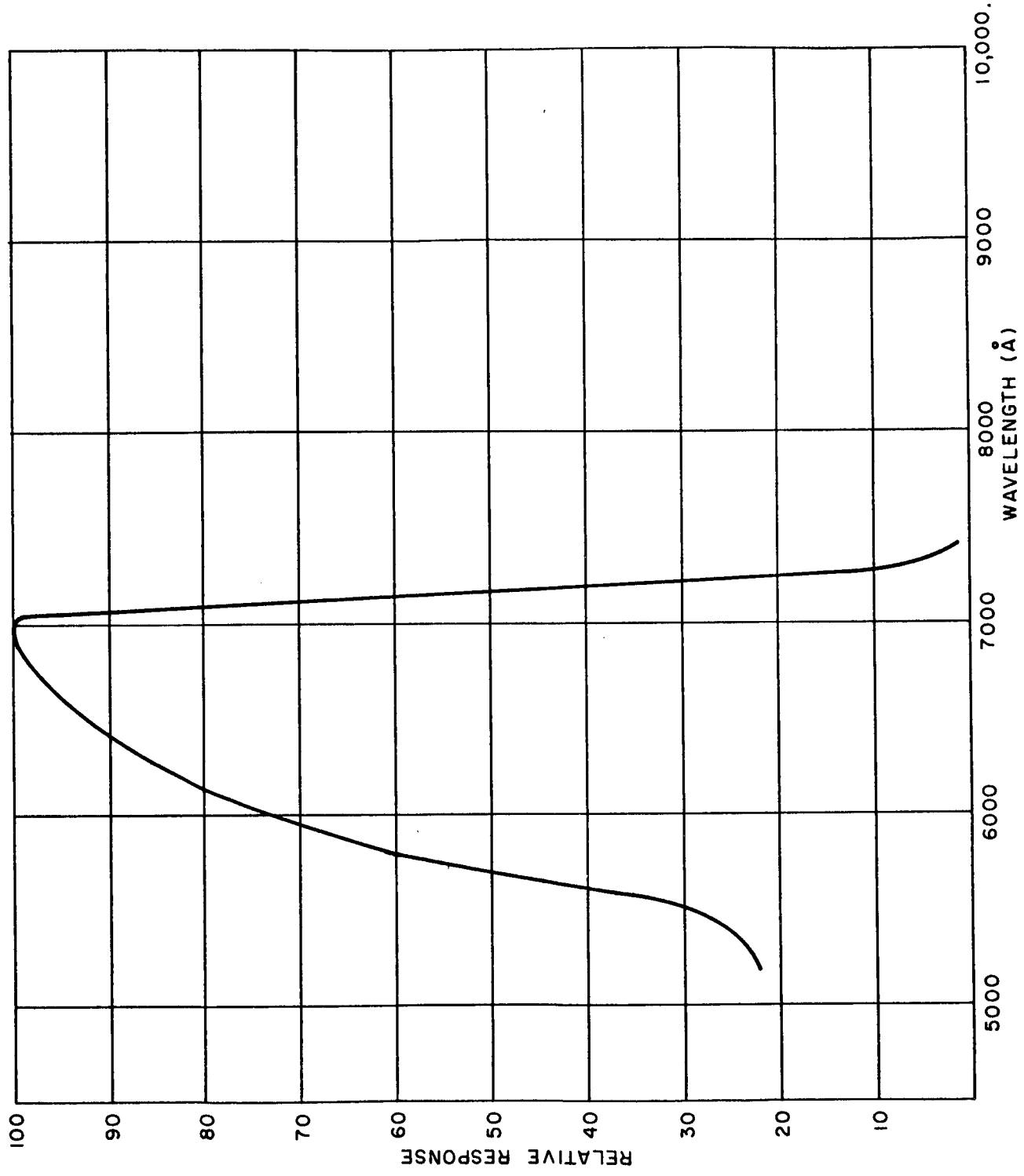


Figure 39

Spectral Response of Sputtered CdSe Photoconductor

Since the actual operation of the image converter depends upon the change in impedance with changing light level, the light response curve of Figure 40 was taken. The so-called dark level of 10^{-4} ft. candles is only a relative point for the log-log scale. The response in the 0.1 to 100 ft. candle region is supra-linear, indicating a high sensitivity.

E. INTEGRATED IMAGE SENSOR MATRIX

1. Array Design

Based upon the circuit design, the design of the integrated array was based upon the following methods of fabrication: (see Figure 41).

a. Diffused plannar diodes on a silicon wafer. SiO_2 protective surface on entire wafer, with gold filled windows cut to contact p-dot on diode.

b. KPR masked platinum electrode, 16 x 16 mils, centered over the diode area. This electrode forms one plate of the capacitor and also one contact to the photoconductor. This process has been discussed in section IV-D-3.

c. Vapor reacted SiO_2 over the entire wafer at a thickness of 1500-2000 Å.

d. A window, 2 x 16, etched in the SiO_2 to allow the photoconductor to contact the base electrode. KPR masking techniques are described in a following section are used.

e. Top electrode of the capacitor, deposited either by metal mask or KPR masking techniques. This platinum electrode is 12 mils wide and extends the entire wafer, contacting 30 intersections. Thus, in addition to serving as the capacitor and photoconductor electrode, it also connects the columns together. (The line runs "into the paper" in this diagram).

f. A photoconductor layer sputtered through a metal mask onto the two exposed platinum electrodes. After firing the photoconductor, the matrix array is completed.

g. Isolation of the rows by scribing and cracking the wafer along its preferred planes. The wafer must then be reassembled into a mechanically connected assembly and the column leads bridged across the gap. This will be discussed in more detail in a following section.

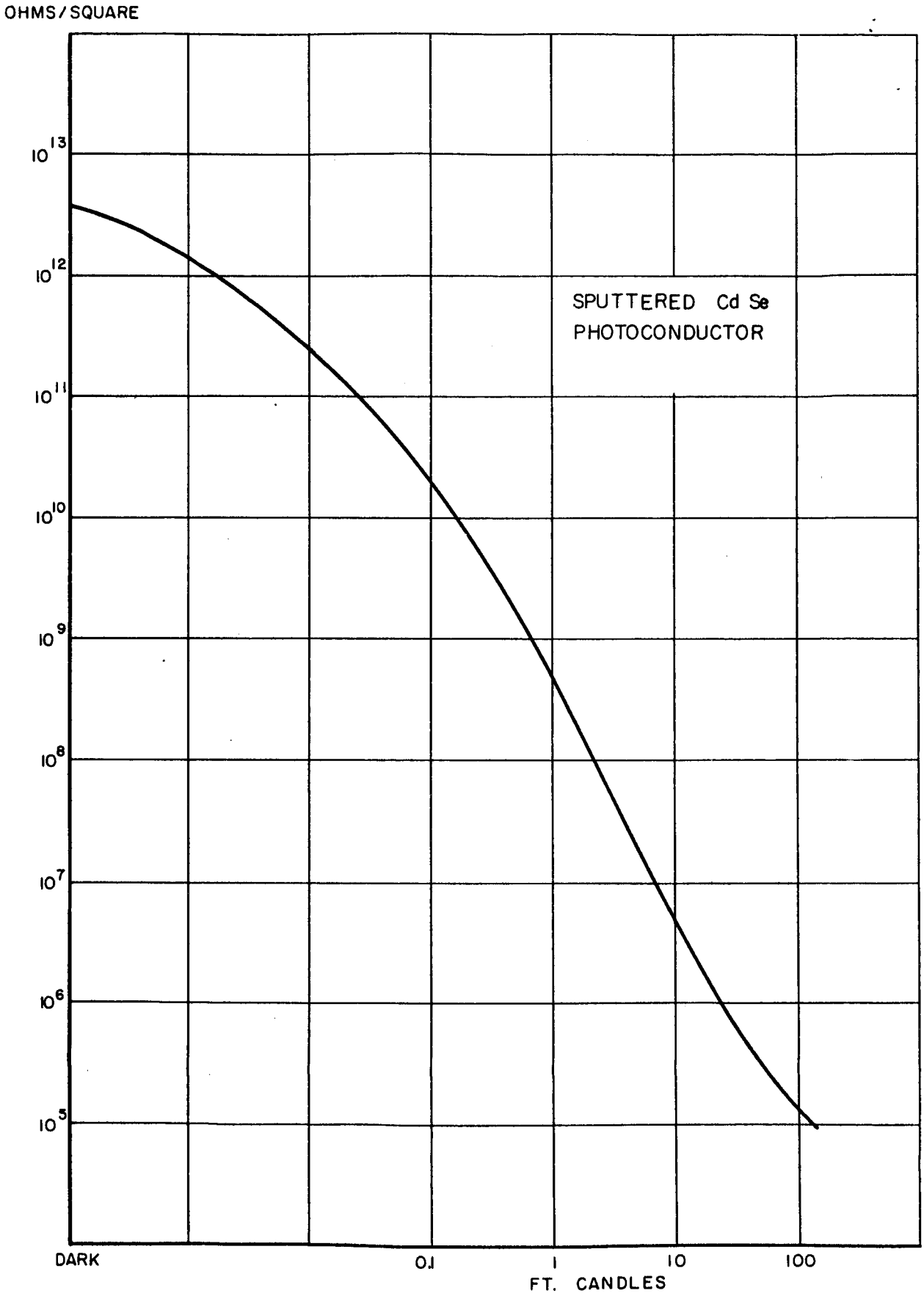


Figure 40
Sputtered CdSe Brightness Response

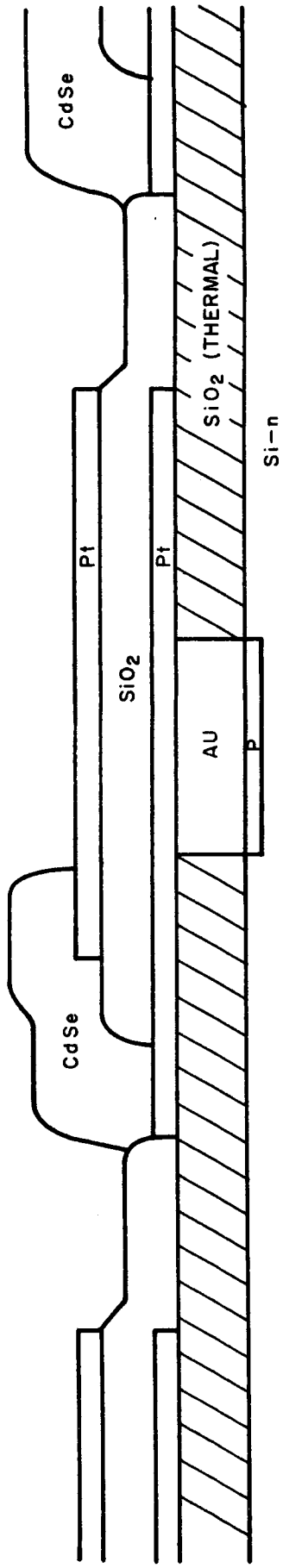


Figure 41

Structure of Image Sensor Matrix

2. Fabrication Techniques

a. Masks

The element size used throughout the development program was a unit area of 20 x 20 mils, 16 x 16 of which was available for device deposition. An initial group of masks were made having only 5 elements, but of appropriate size and also having fan-out leads to facilitate testing. These are shown in Figure 42.

The masks for the full 30 x 30 array are shown in Figures 43 and 44. The four masks of Figure 43 are: top left: 16 x 16 mil square area to form first platinum electrode; top right: 6 x 16 areas defining the photoconductor; bottom left: 12 mil strips forming the column connections, and also the top contact to the capacity; and bottom right: 2 x 16 mil openings to control etch pattern in the deposited SiO_2. Figure 44 shows metal masks made from these negatives.

b. SiO_2 Etching Procedures

Because of the apparent differences in structure between plasma deposited SiO_2 and thermally grown SiO_2, it was not expected that the etching rates of the two films with a given etch would be the same. This prediction was quite correct; the plasma deposited SiO_2 etches much more rapidly than its thermally grown counterpart. Several experimental etching solutions were tried using HF diluted with various portions of H_2O and NH_4F. The HP content seemed to be the only actual factor affecting the etching rate. The resultant etching rates of plasma deposited SiO_2 with different HF concentrations is shown below. The etching rates were determined by observing interference color band shifts as a function of time and hence represent only approximate values.

Vol. of 48% HF	Etching Rate
5%	17 Å/sec.
10%	30 Å/sec.
20%	100 Å/sec.

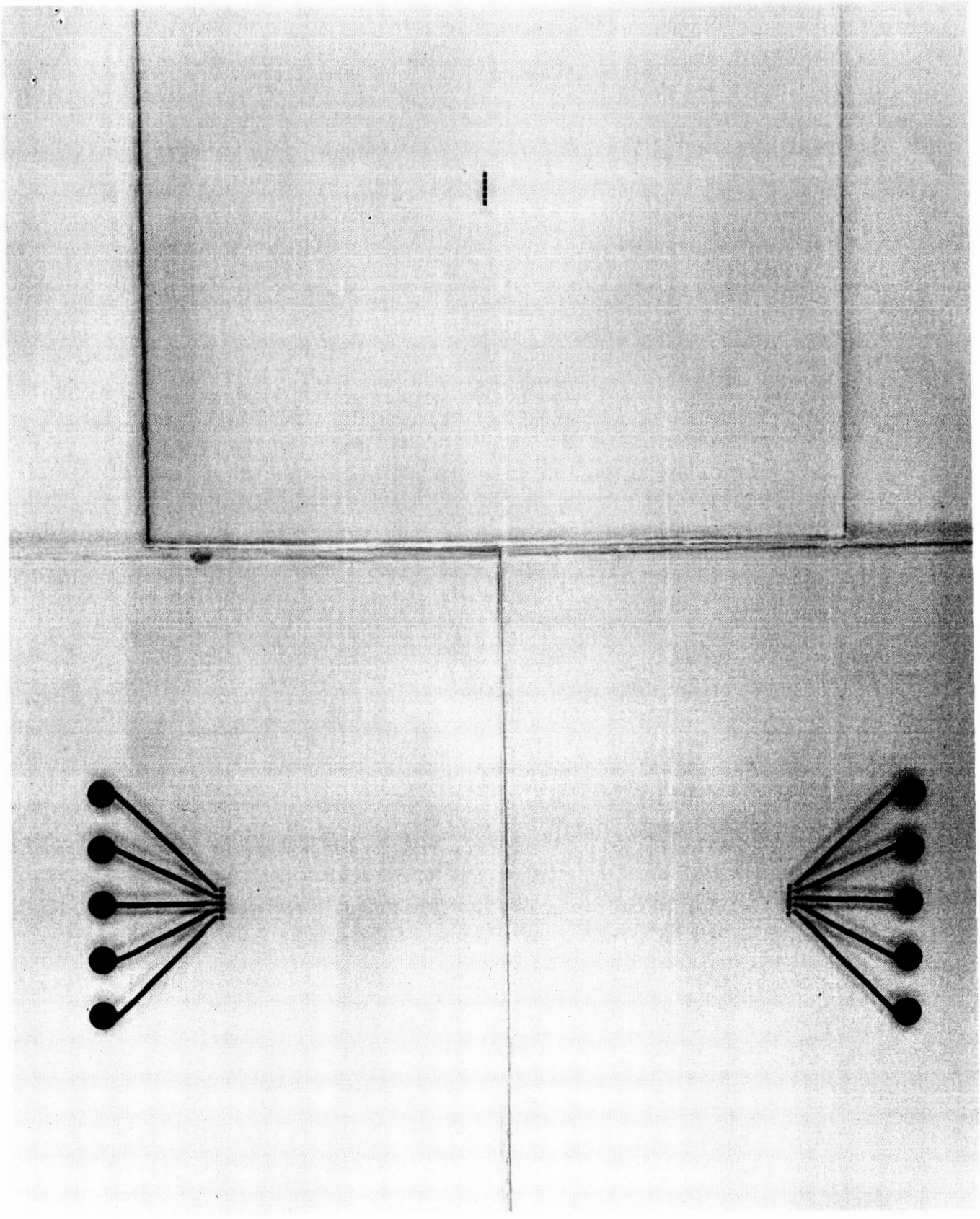


Figure 42

Test Array Masks

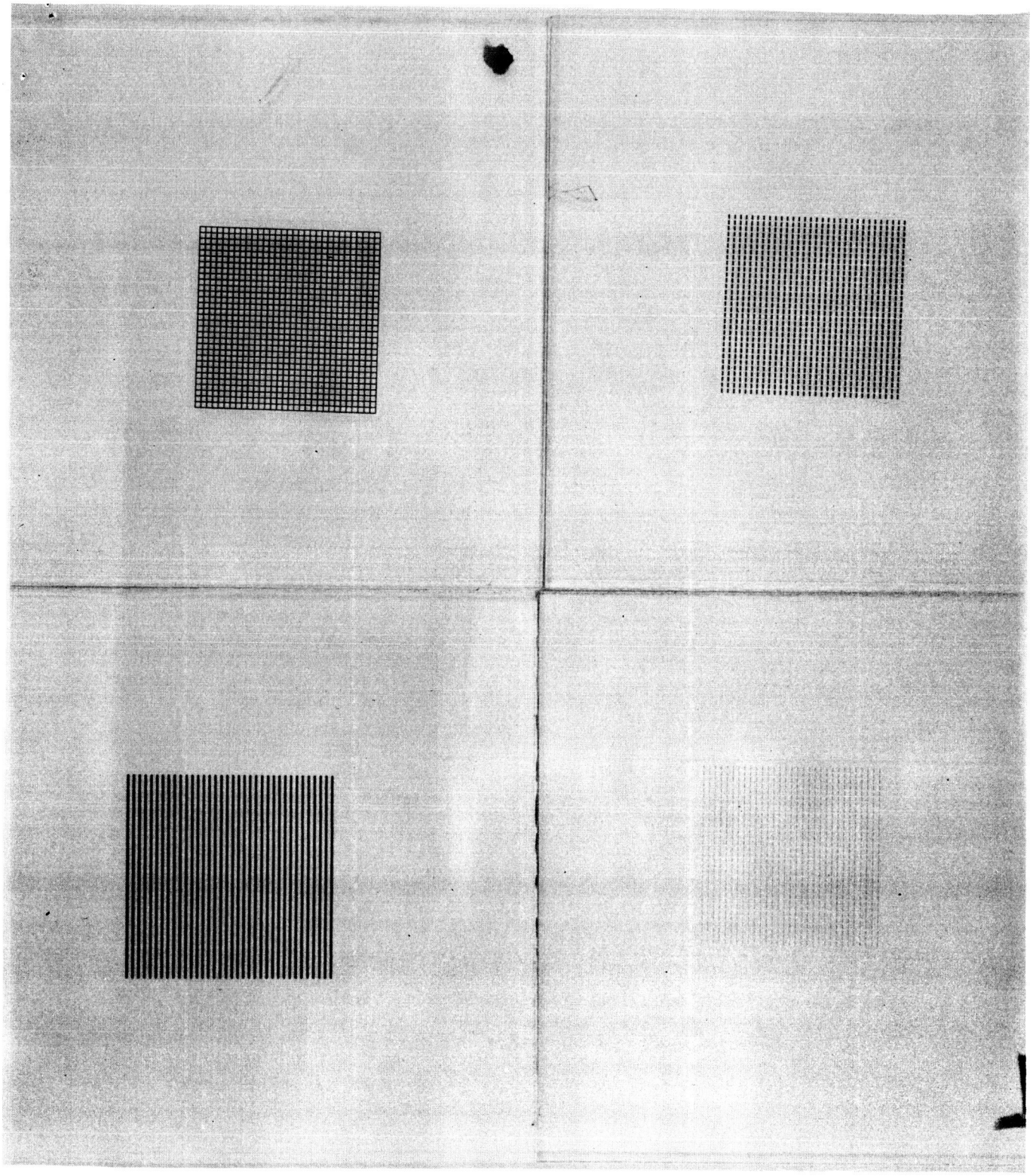


Figure 43

Final Array Masks

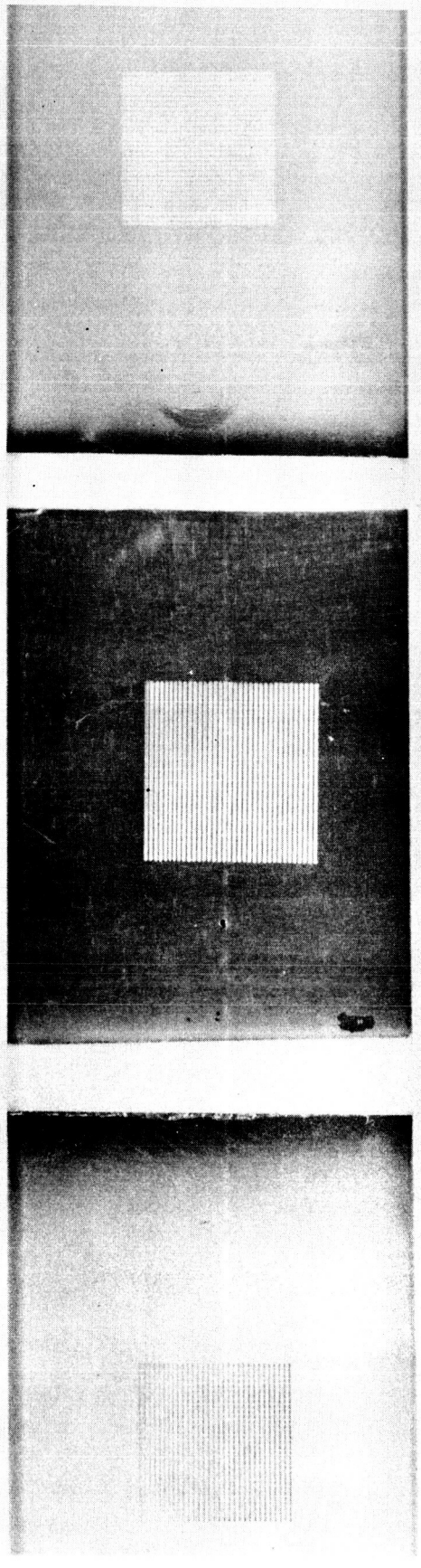


Figure 44
Metal Masks for Final Array

The first etching experiments with the image converter structure were performed using a silicon substrate with 16,000 Å of thermally grown SiO_2 on its surface. Over this a thin platinum film was sputtered in the form of an electrode pattern. A 1200 Å SiO_2 layer then was deposited over the entire structure. A photoresist layer was then processed over the SiO_2 to provide windows through the resist layer directly superimposed over the platinum electrode areas. The sample was etched for one minute with intermittant agitation in an etching solution containing 10% by volume of 48% HF. As soon as the SiO_2 was removed and the platinum electrodes were exposed to the etchant, flashes of platinum floated to the surface. Apparently the sputtered platinum films had sufficient porosity so that the HF quickly penetrated them and reached the underlying thermally grown SiO_2 layer. The etching action underneath the electrode was sufficient to lift the platinum.

All other attempts to etch SiO_2 deposited over sputtered platinum layers were unsuccessful even though several combinations of etch formulations and etching times were used. It was, therefore, decided to use evaporated films for which the anticipated porosity was considerably reduced. Successively evaporated thin layers ($\sim$400 Å total thickness) of nichrome and platinum were used on a thermally grown oxide layer, 16,000 Å in thickness. These metal layers stood up without any apparent lifting to an 8 minute exposure in a very strong (20% by volumn of 48% HF) etch. This procedure was subsequently used to etch 2 mil by 14 mil windows through plasma deposited SiO_2 covering these evaporated metal films with great success. A photograph of one of these windows on a 16 mil platinum square is shown in Figure 45. Some undercutting was observed but this was the fault of the photoresist processing and could be improved by baking the photoresist at a higher temperature.

c. Completed Array

The sequence of photos of Figure 46 indicate the process steps of fabricating the complete wafer. In the upper left is the original silicon wafer with the 4.2 mil diodes on 20 mil centers.

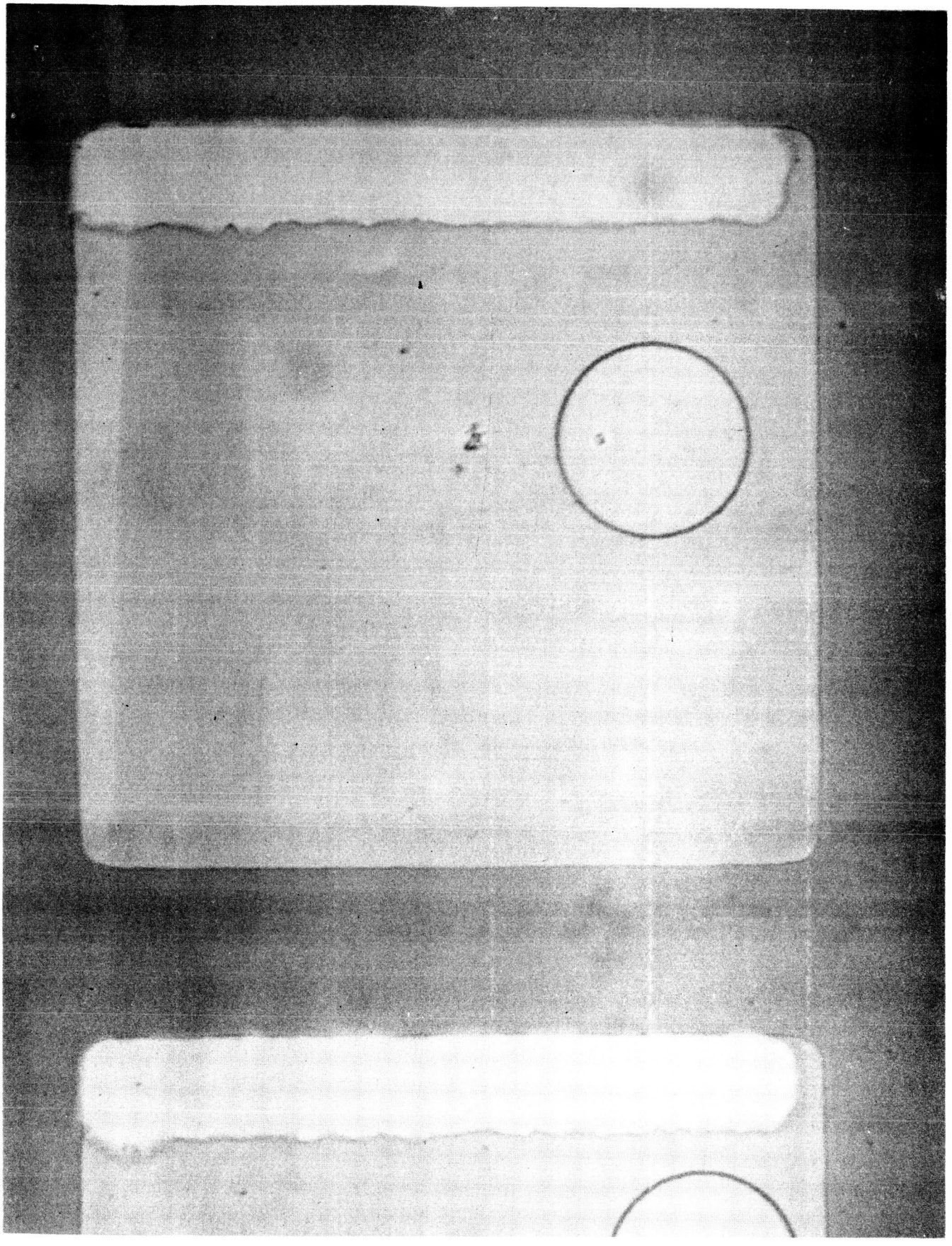


Figure 45

Etched SiO_2 Window

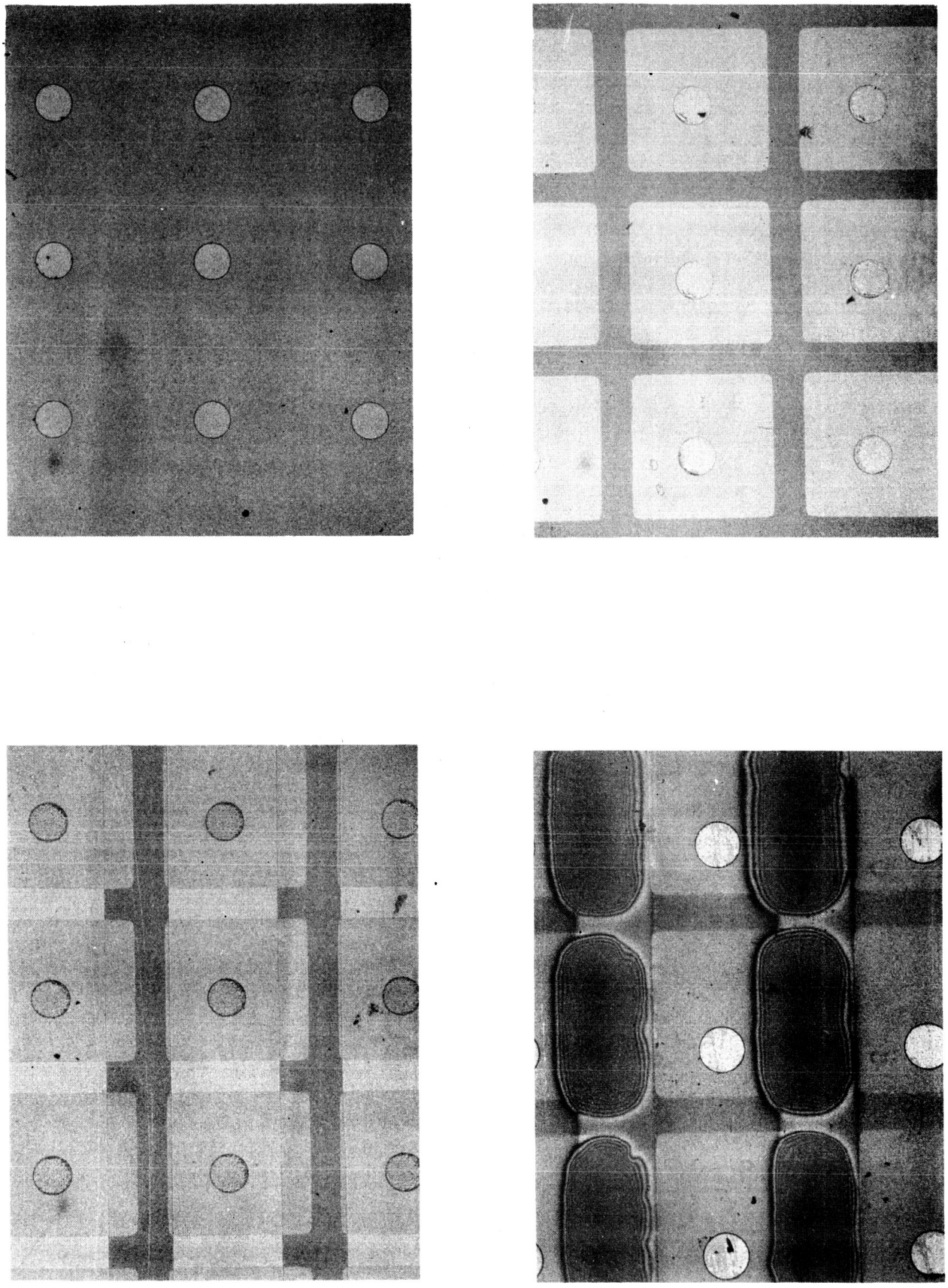


Figure 46

Fabrication Steps for Image Sensor Matrix

The upper right shows the addition of the 16 x 16 mil platinum electrodes on the surface of the wafer. Several surface imperfections are evident which have deleterious effects on the capacitor. The picture appears identical after the deposition of the SiO_2, so that step will not be shown.

The lower left photo shows the addition of the 12 mil top electrode spanning the entire column. The SiO_2 has already been deposited, so each 12 x 16 mil area under this conductor is a capacitor.

The final assembly is shown in the lower right. The large dark area is the CdSe. It is evident that a great deal of undercutting occurred during evaporation by the size of these deposits, since the mask size was only 6 x 16 mils.

3. Problems Encountered and Required Development

It was not possible during this program to construct an electrically operable image sensor matrix. The two areas of difficulty were the capacitor leakage and the photoconductor edge definitions.

Although it was possible to fabricate good capacitors on glass substrates, as well as on blank SiO_2 coated silicon wafers, it was not possible to fabricate a good capacitor on the actual diode array. The solution to this difficulty is believed to lie in the edges presented to the dielectric by the presence of the diode contact window. Although the diagram of Figure 41 does not show the scale properly, it will serve to describe the problem.

In the diode processing the SiO_2 layer is grown over the entire wafer to a depth of 16,000 Å. A window is then cut above each diode and subsequently filled with gold. It does not, however, as indicated in the figure, form a flat surface. Instead there is a cavity that extends 5000-10,000 Å below the SiO_2 surface. This cavity appears to be extremely deep to the subsequent layers of platinum and vapor reacted SiO_2, which are only in the order of 1000 Å and 2000 Å thick respectively. It is thus quite probable that a near breakthrough occurs at the edge of the cavity, causing the low leakage resistance measured for the capacitor (in the order of a few k-ohms). Since the diode is 4.2 mils wide, and the top electrode 12 mils wide, it was not possible to avoid the diode ridge with the capacitor.

Several solutions are proposed to this problem, each of which would circumvent this sharp surface discontinuity.

(a) Make the diode much smaller so as to be able to place it entirely under the area outside the capacitor. An additional saving here might be the elimination of the need to etch the windows in the SiO_2, since the surface discontinuity would serve this function of contacting the photoconductor.

(b) Reverse the structure to place the capacitor-photoconductor structure on the reverse side of the diode. This was mentioned earlier in conjunction with the capacitance developed between the 16 x 16 mil electrode and the silicon wafer, the thermal SiO_2 acting as the dielectric. With this structure on the back side of the wafer, different row-column isolation would have to be employed. There is no problem to scribe and cut the array into individual pieces, as this is a standard manufacturing technique used with present diode and transistor structures. This approach would be acceptable down to sizes of about 7 mil strips or 150 lines/in.

Photoconductor edge definition limitations are observed on the photograph of Figure 46. This deposition was performed by sputtering through a metal mask. Although the basic approach is not new or unique to this project, the resolution is high for most metal masking techniques, considering the registration requirements. It is also observed that as long as the photoconductor does not contact an adjacent photoconductive cell or adjacent column line, there is no difficulty.

Additional development in this area is necessary to determine the best possible method of masking the CdSe. An additional approach was briefly tried, but without immediate success; it involves the photoresist masking of the areas to deposit the CdSe, much as is done with the platinum. Successful control of either of these processes would eliminate this problem.

4. Array Interconnections

From the earlier discussion of the circuit design and the array design, the task of isolating the elements from each other is presented. This isolation refers to the separation required between the individual rows and columns.

One isolation is afforded by the deposition of the 12 mil top conductor. The second isolation is required because the silicon wafer used as a substrate is highly conductive and thus interconnects all the diodes.

The technique proposed for the 30 x 30 matrix involved the scribing and cracking of the wafer into 20 mil strips and remounting these into a single structure; monitoring a separation between the rows.

Although the scribing and cracking presented no problems, the remounting of the devices was somewhat more complex. In the final assembly, an acrylic holder was fabricated, having 2 mil ridges between the silicon strips. The strips were cemented via a lead through the bottom of the holder.

Since the integrated structure was never fully completed, the step of completing the column connections was never actually performed. The technique proposed, however, utilized a photoresist to form a continuous top surface over the holder and strips. The photoresist is then exposed and developed to gain access to the 12 mil conductor on the strips. A second evaporation will reconnect these column lines, completing the matrix.

V. FEASIBILITY DEMONSTRATION MODELS

A. DELAY LINE MODEL

An image converter model, consisting of an 81 element photosensor matrix, two 9 tap ceramic delay lines and supporting microelectronic sync circuitry, has been constructed to demonstrate tapped delay line scanning. Figure 47 is a photograph of the mounted model. The components that make up the model are described in some detail below.

1. Photosensor Array

The 81 element array uses the charge storage principle of image scanning, previously described, consisting of diode, photoconductor and capacitor elements. The matrix interconnection scheme described in Figure 8 previously is used here. The array and delay line orientation in the model is identical to Figure 8, such that line 2 is grounded.

The array element values were chosen to be consistent with the delay line scan from rates expected. A Clairex CdS photoconductor, type CL602 was selected for its 100 K ohm resistance at 30 ft candles illumination, and about 10 megohms at 0.1 ft candle. A charge storage capacitor value of 470 pf yields an appropriate time constant of 47 μs at 30 ft candles. The diodes used are GE types SD300 and IN4443, identical except for encapsulation. Both types are silicon epitaxial units, without gold doping, as used in the 30 x 30 fabricated array. A few gold doped diodes, GE type IN3605, have been substituted for comparison purposes reported below. Each photoconductor and capacitor are soldered together and connected with the diode to the conductor matrix via the transistor socket soldered at each conductor intersection. A bakelite plate is used to hold the photoconductors in place.

2. Delay Line Scanner

Both ceramic lines incorporate the most recent improvements discussed previously. GE427AA ceramic is used, with electroless Ni electrodes. The material has been poled only in the regions directly under the electrodes.

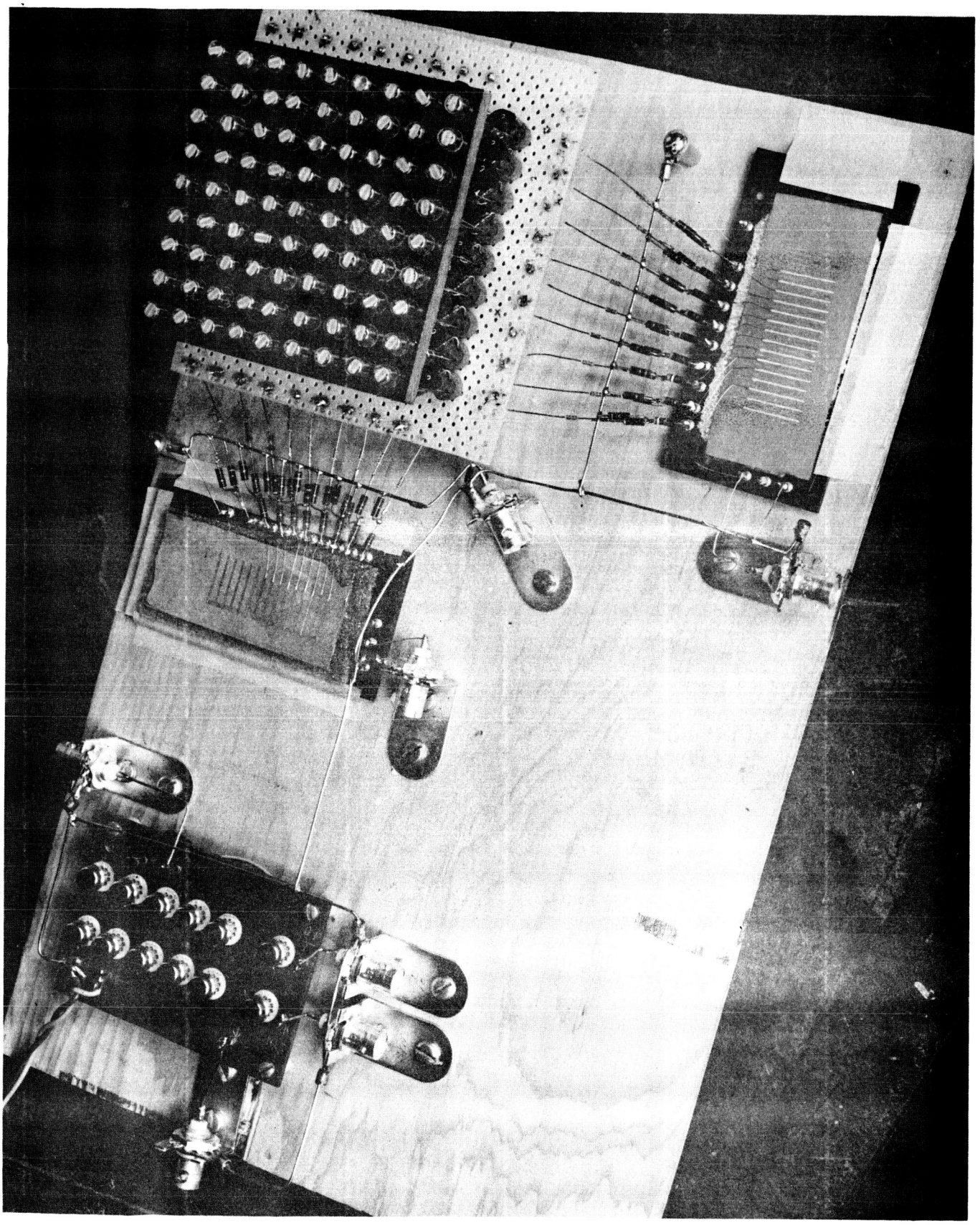


Figure 47
Delay Line Scanned Image Converter Model

The edges of both lines have been scalloped to disperse the reflected wave. The electrodes are spread on 120 mil centers, which is twice the original spacing, to obtain a suitable frame rate. Thin electrodes have been built up with air dry silver plate. The drive electrode of line 1 is located at the ceramic edge; delay line 2 is driven from the third available electrode. The lines are mounted on bakelite bands with styrofoam pads.

These delay lines require a 60-80 volt drive pulse to obtain a 1.0 to 1.5 volt output. The output pulse delay is equal to 0.84 μsec/tap.

3. Compensating Networks

A passive network of three resistors and an isolating diode connect each delay line tap to a matrix conductor. This network is used to provide a constant output voltage from tap to tap. The resist values were chosen as described previously. Isolation diodes without gold doping (GE IN4443 and SD300) are used. The video output voltage is developed across a 100 ohm resistor between ground and the common bus bar of delay line no. 1.

4. Synchronizing Circuitry

The clock driver sync operation scheme described earlier is used in this model to trigger the external pulse generators. Motorola microcircuits of the same type used for microelectronic scanning, were selected to duplicate the dividing circuits of Figure 10. Two additional circuits, not shown in the figure, are used to supply a bias voltage and to shape the clock signal input. The circuits increase are listed below.

(8) J-K Flip Flop: Motorola No. 358
(3) 3 Input Gate: Motorola No. 356
(1) Bias Driver: Motorola No. 354

The clock pulse repetition rate required equals 1.19 mc, corresponding to the tap delay of 0.84 μs/tap. The horizontal rate is one tenth this rate, or 119 KC. The frame rate equals one ninth of the horizontal rate, or 13.2 kc. This corresponds to 75.5 μsec between successive interrogations of the same element, correctly related to the 47 μsec time constant calculated for 30 foot candle illumination.

5. Test Results

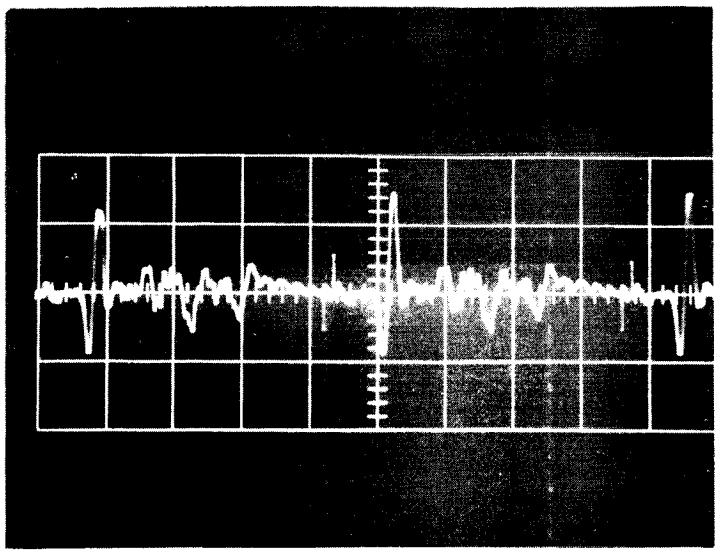
The components described above were interconnected and operated with the required external power supply, clock signal source, and pulse generators. Waveforms of the delay line output and video output voltages are given under various conditions. A more detailed description of operating conditions is given in the operating instructions.

Figure 48 shows the output waveforms of both delay lines operating in the model. An 80 volt input pulse is applied from a 50 ohm source with 0.4 μsec pulse width, and 20 ns rise and fall time to each line. Output pulses shown are observed at the output of the compensating network. The pulses are approximately 0.2 μsec wide at 50% amplitude, and 1.5 volts. The first pulse in each photo is interrogating the matrix; its reduced amplitude is due to the voltage drop across the compensating resistors. Note the acoustic reflection noise amplitude and the differentiated drive pulses. The effect of this noise will be observed in the video wave forms below.

Figure 49 shows the video output obtained from scanning an illuminated matrix row. The pulse amplitudes are typically 150-200 millivolts with approximately 0.15 μsec pulse width at 50% amplitude. The pulse separation of 0.84 μsec would be reduced to 0.92 μsec, if the delay line taps were spaced at 60 mil centers. The negative overshoot present is due to stored charge in the diodes without gold doping.

Figure 50 shows the video output obtained from scanning the first line of the 81 element matrix. Elements 7, 8 and 9 at the end of the scanned line have diodes with gold doping and exhibit no negative overshoot. The presence of the overshoot has little effect upon the illumination characteristics and would ordinarilly be clipped off when a black level is established in subsequent video processing. Element 7 has failed through mechanical handling of the matrix.

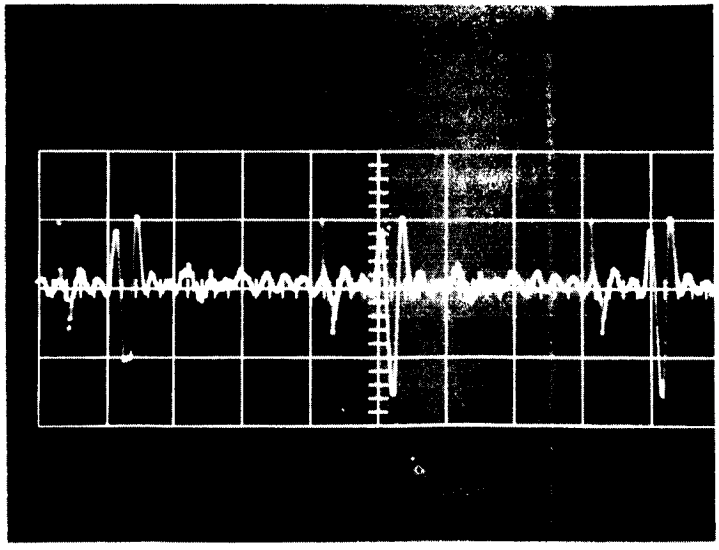
Waveform (a) represents all matrix elements illuminated. Wave form (b) shows the effect of covering elements, 2, 4, 6, and 8. In waveform (c), the remaining noninterrogated elements have been covered. For proper image converter operation, waveform (b) should be identical to waveform (c). The



(a) Output Voltage,
Delay Line no.2
(grounded)

2.0 μsec/cm,

1.0 volts/cm



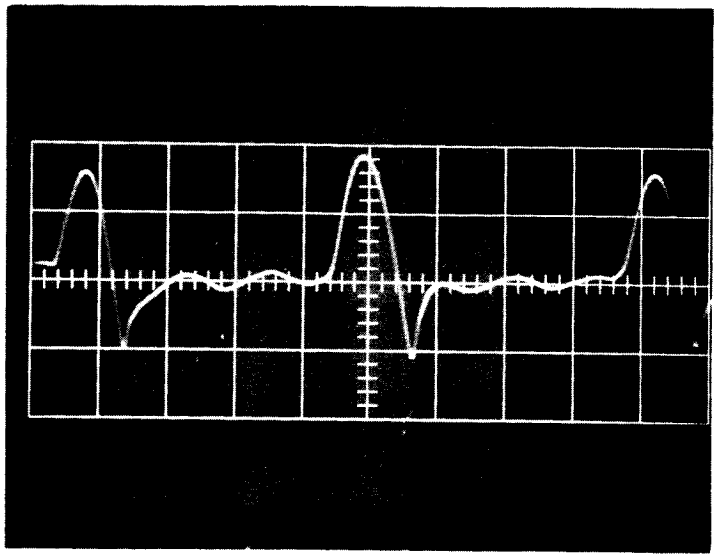
(b) Output Voltage,
Delay Line no.1
(floating)

2.0 μsec/cm,

1.0 volts/cm

Figure 48

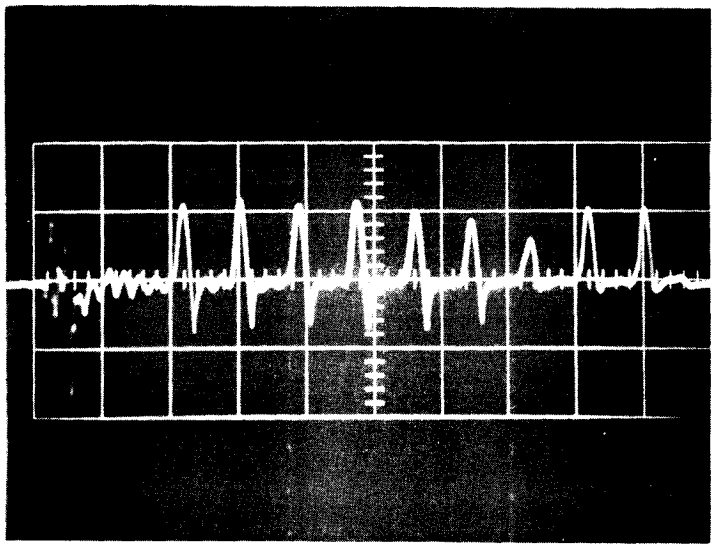
Delay Line Scanning Voltage



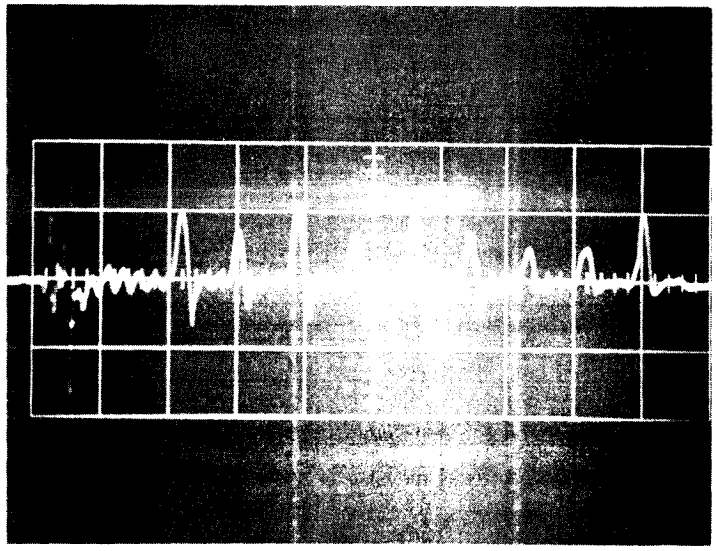
0.2 μsec/cm, 100 mvolts/cm

Figure 49

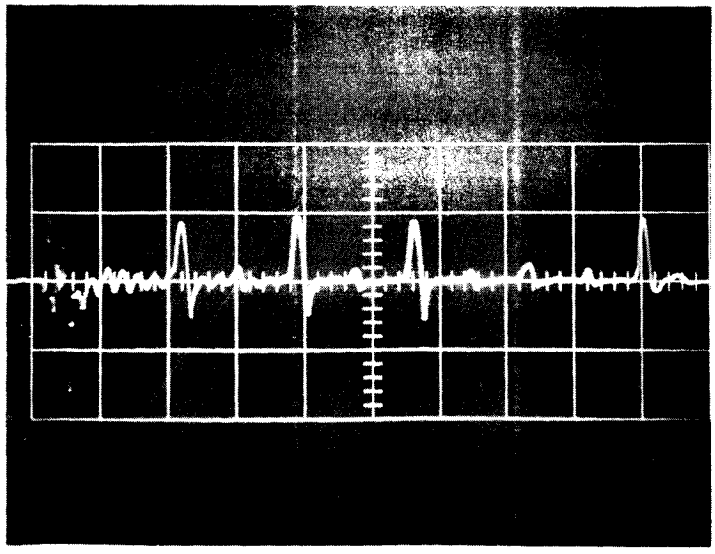
Video Output Pulse Detail



(a) All matrix elements illuminated. (Element No.7 has failed.)



(b) Elements no.2,4, 6,8, no illumination. Other elements illuminated.



(c) Elements no.1,3, 5,9 illuminated. Other elements, no illumination.

All photos 1.0 μsec/cm

0.2 volts/cm

Figure 50
Video Output, First Line of Matrix Scanned

difference is due to conduction through the noninterrogated elements that are in common connection to elements 2, 4, 6, and 8. This leakage appears to be inherent in coincident voltage selection without reverse bias.

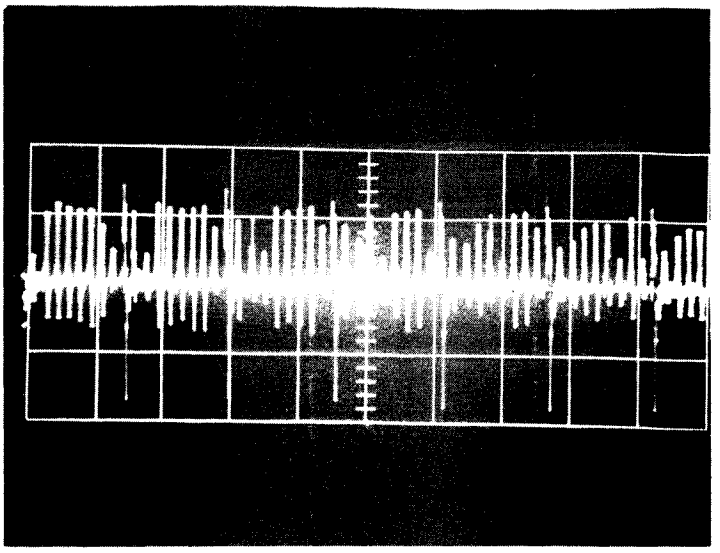
Note that the effect of the delay line acoustic noise is negligible while the drive pulse coupling is clearly visible.

Figure 51 shows the first six lines of the nine line matrix being scanned continuously. The drive pulse of the floating delay line (1) is capacitively coupled into the output and must be eliminated for proper operation. Waveform (a) is the video output for all matrix elements illuminated. The variation in pulse amplitude is due to the use of compensating network values not matched to a delay line that was substituted for a broken line. Waveform (b) shows the result of illuminating the first line only. Leakage c currents through the elements of the first line are evident in the subsequent lines.

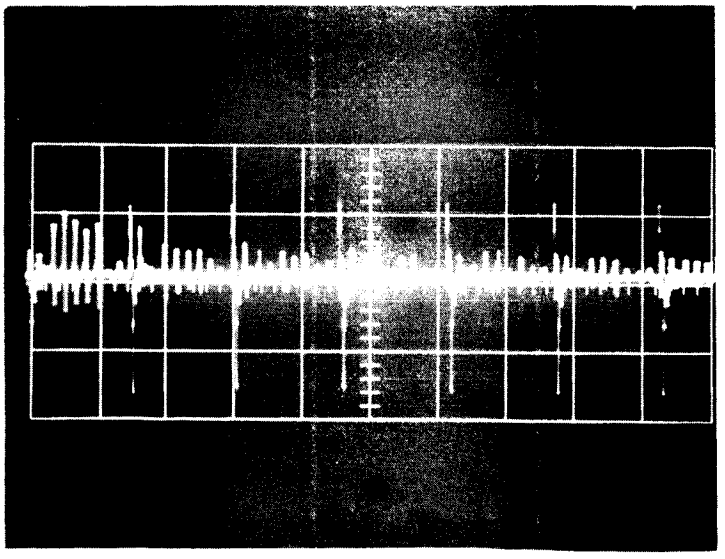
B. MICROELECTRONIC SCANNER MODEL

The described matrix equivalent circuit elements, Figure 24, were demonstrated with V_D = 5.5 volts, V_c = 5 volts, and V_R = 5 volts. Saturation current pulses (matrix capacitor 95% discharged before each interrogation) observed were 10 MA peak and 50 μsec wide (see top of Figure 52). Hence, a maximum bit rate available for transmission is of the order of 20 megacycles per second with the demonstration model. The frame time, of course, is limited by the light sensitivity required for given matrix discharge rates. In practice the matrix interrogation rate was 1/4 μsec or 1/2 μsec (switch selected) to match the counting circuits constructed to a standard broadcast television monitor.

Although the 900 matrix elements are not sufficient to fill a conventional TV raster completely, the pulse width and pulse repetition rate for a single element are appropriate for display in a conventional TV format. The matrix elements are grouped electrically to occupy a continuous 1/8 of a horizontal scan and a continuous 1/8 of a vertical scan; forming a block in the upper left hand corner of the display. An optional switch-selected modification of the scan will expand the display spread. The display elements



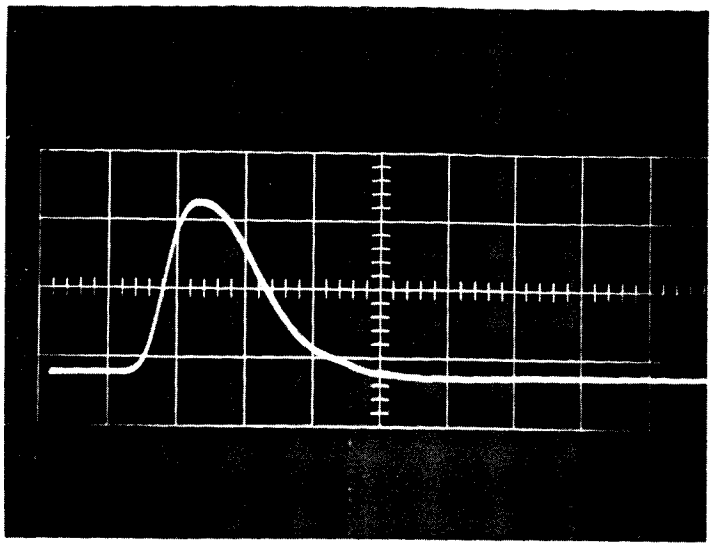
(a) All matrix elements illuminated.



(b) First line of matrix illuminated. Other elements no illumination.

both photos 5.0 μsec/cm
0.2 volt/cm

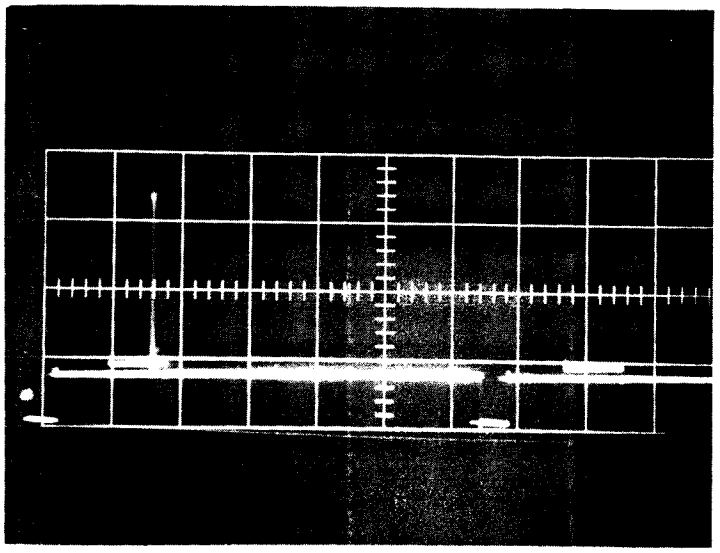
Figure 51
Video Output, First Six Lines



5 MA/cm

40 η sec/cm

Matrix Current

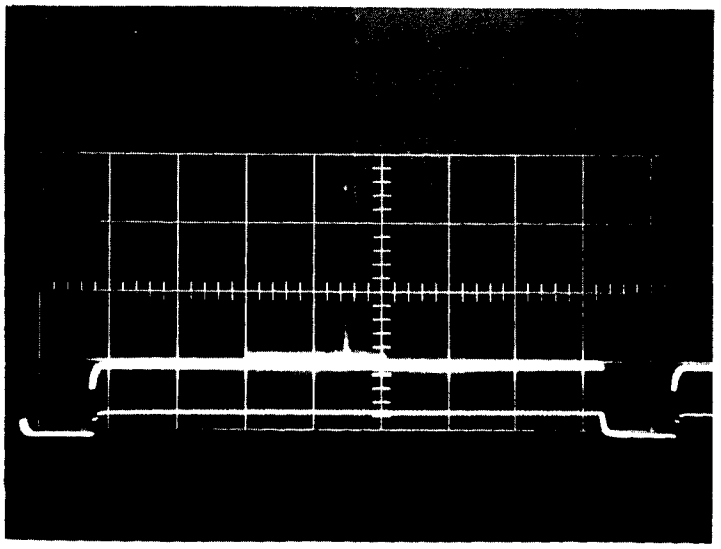


Output

2 V/cm

20μ sec/cm

Horizontal Inverval



Output

2V/cm

2 millisec/cm

Vertical Interval

Figure 52
Microelectronic Scanned Array-Waveshapes

are twice this spacing apart for detailed examination, but maintaining the individual pulse width and pulse repetition rate. The output amplifier combines the sync generated by the micrologic to form a one volt peak to peak composite video signal to drive a terminated 75 ohm transmission line. For simplicity, the output transistor collector DC return is through the remote 75 ohm termination, as the DC path must be completed. The use of low impedance circuits, and the high matrix output combine to give a simple output amplifier without requiring compensating circuits. External gamma correction can be applied if required for a given application. Figure 52 shows output waveforms which detail the sync and blanking pedestal output in the vertical and horizontal intervals. The synchronizing signal approximates industrial quality sync, but is not as complete as broadcast quality sync since no equalizing pulses are formed. This does not directly influence operation of the image converter, only the display monitor. Independent horizontal and vertical synchronizing signals are generated and can be amplified and used to drive the monitor directly if required.

Although the output drivers are constructed using discrete components, and the size and type of components were chosen for the demonstration model on the basis of availability and performance, future units can be designed around monolithic integrated microcircuit techniques entirely. Such circuits can be built according to mil specs and since the circuit complexity for a large matrix is of the order of a small digital computer, similar failure rates can be expected. The use of redundant circuitry can effectively reduce failures. In addition, the logic configuration can be chosen to confine failures to small segments without impairing the overall scan circuit operation.

The same 9 x 9 element photosensor matrix array described in connection with the delay line scanner was driven by the microelectronic scanner. The photograph of Figure 53 was obtained utilizing an optical mask. Light levels of 0.02 ft-candle illumination was sufficient to obtain a display on the TV monitor. The mask and photocell array are shown in Figure 54.

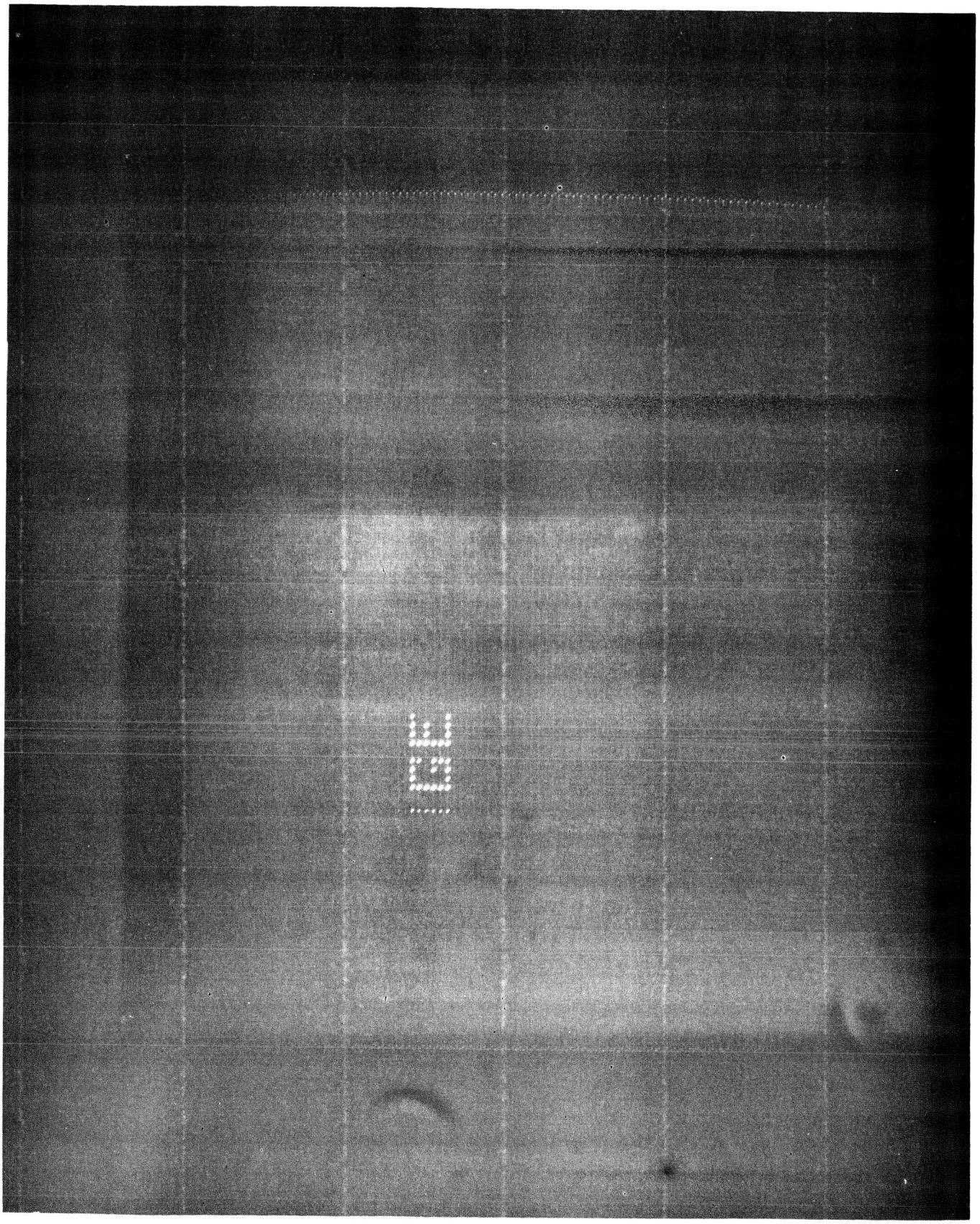


Figure 53
TV Monitor Display of Scanned 9 x 9 Array

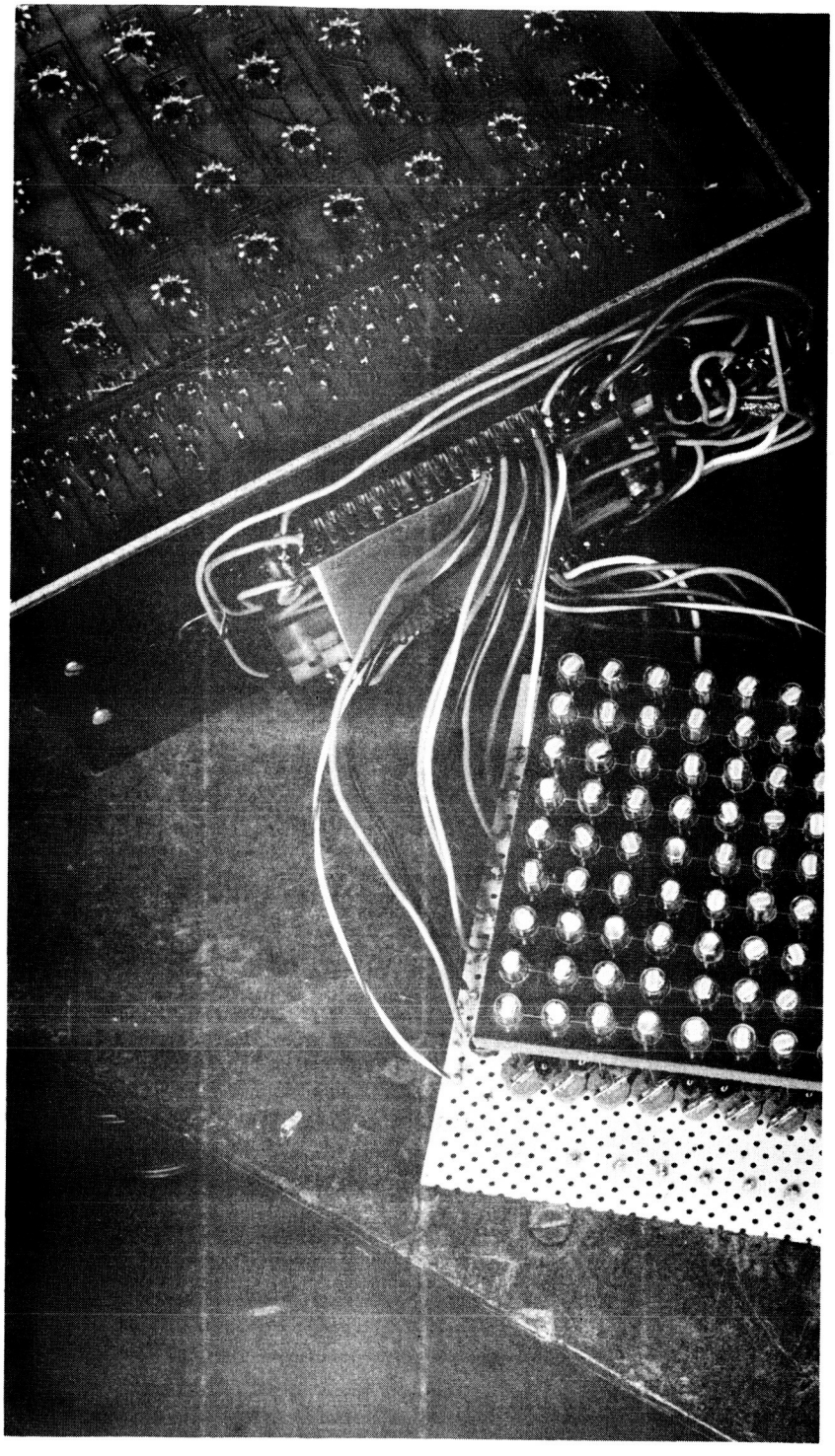


Figure 54

Microelectronic Scanner and 9 x 9 Array

VI. HIGH RESOLUTION IMAGE DETECTORS

A. COMPARISON WITH ULTIMATE GOALS

The ultimate goal of the project was stated to be a solid state image converter with a cross section of four square inches capable of 600 to 800 lines of resolution. With the present status of development, a more detailed estimation of the overall potential of reaching this goal can be made.

Two criteria must be met by the overall device; it must be capable of delivering an output signal in excess of the system noise, and it must be amenable to fabrication techniques.

From the discussion of section III-B, the role of the shunt paths through the matrix became increasingly important as the number of elements is increased. For a signal-to-noise ratio of one, that is, the shunt path through the matrix is equal to the capacitor charging

$$C_{pc} = \left(\frac{n-1}{2}\right) C_d$$

For the design goal of 600 total lines this requires

$$C_{pc} > 300 \quad C_d$$

Using the minimum realizable junction capacitance of 0.1 pf, (as obtained in pin varactor diodes) the charge storage capacitance must be greater than 30 pf to provide a detectable output. Placing the capacitance within the area dictated by the 300 lines per inch requirement, requires a capacitance of 5 $\mu f/in^2$ to achieve the 30 pf. Operating at a signal-to-noise ratio of 3, raises the requirement to 15 $\mu f/in^2$.

This level is well above the 0.2 - 0.5 $\mu f/in^2$ obtained from the SiO_2 dielectric used in the present phase of the project. Use of high dielectric materials is an obvious necessity to obtain the specified resolution and density. High performance thin film capacitors have been fabricated in the laboratory having 1 $\mu f/in^2$ and it is believed that a value of 3 $\mu f/in^2$ can be obtained for a capacitor having the required breakdown strength and leak-

age. This, however, is still well below the required capacitance for a high resolution system.

It is important to note that the circuit analysis does not specify the type of capacitance and, therefore, is a general analysis of a matrix image converter. This means that the n-p-n junction detectors described in section III-A are also limited by the same considerations, as is any sensing element that is dependent upon a diode for its isolation.

The solution of these problems was pointed out in the Major Conclusions of the first final report, namely a slightly reduced resolution and number of lines.

There are, however, a number of approaches which circumvent this limited operation. Using as the original specifications:

A. 600 lines
B. 300 lines/in
C. 2 x 2 inches

the following three capabilities are described. On each case the assumption of a 3 $\mu t/in^2$ capacitance and a 0.1 pf diode is made, and in each case one of the original goals is maintained, (indicated by an asterisk).

	I	II	III	
A:	600*	120	380	lines
B:	150	300*	190	lines/in
C:	4 x 4	0.4 x 0.4	2 x 2*	inches

While the total objective of a high resolution matrix does not appear to be realizable with present components, each of the alternative approaches would fulfill certain areas of application. Indeed it is a desirable feature of the matrix scanned image detector that it is capable of operating over a wide set of geometrical patterns.

B. REALIZABLE IMAGE CONVERTER SYSTEMS

Although the alternative scheme III is simply a reduced resolution model of the original goals, approach I and II offer the possibilities of achieving the desired goals in a modified system approach.

Since we have concluded that model I and model II represent the limiting size of the image sensor matrix that will yield an output signal from both circuit and materials considerations, it remains a system problem to achieve the overall goal. Two approaches are presented here; these designs have been developed during the program as a result of refined calculations and measurements of the matrix parameters.

1. Using scheme I, namely a reduced resolution of 150 lines/in, a total detector size of 4" x 4" is required to accommodate 600 lines. The main problem here is to expand the incident image onto the larger screen. To do this, a reflecting optical system can be utilized to enlarge the image to the proper size.

In making this optical enlargement, the incident intensity will be reduced by the ratio of the areas, or a factor of four in this case. However, as the matrix described in section III was sensitive to incident levels of .02 ft-candles, the enlarged area image detector would be sensitive to levels of .08 ft-candles, an order of magnitude below the goal of 1.0 ft-candle.

If even larger areas can be tolerated for the sensor surface, a much greater number of lines can be accommodated. For example, at a density of 125 lines/in, 1000 lines can be utilized in an area of 8 x 8 inches.

2. The second system organization of a high resolution image converter involves the elements of scheme II. The resolution of 300 lines/inch limits the matrix to 120 lines because of the signal-to-noise ratio. If we consider the possibility that the total image sensor plane may be subdivided into small matrices such as that of II, then a complete image sensor of the desired size and resolution can be achieved.

The system organization is explained with the aid of Figure 55 . The column driver consists of a single pass ring counter shifting at a rate determined by an external clock. The ring counter responds to a single start pulse and steps through its entire length, at which time it stops and is ready to accept another start signal. The ring counter has one stage for each column in the submatrix and produces a drive pulse for that line.

The row driver consists of a single stepping ring counter driven by the same start pulse as the column driver. Thus when a start signal is applied to one of the submatrices, the row is stepped one position, and all the columns in that matrix are scanned. During this scanning an output is generated in that one submatrix only and it corresponds to the particular row scanned.

For the 3 x 3 submatrix grouping of Figure 55 where each submatrix consists of m rows and m columns, the system operates as follows:

pulse	A	scan	row	A-1
"	B	"	"	B-1
"	C	"	"	C-1
"	A	"	"	A-2
"	B	"	"	B-2
"	C	"	"	C-2
	.			
	.			
	.			
"	A	"	"	A-m
"	B	"	"	B-m
"	C	"	"	C-m
"	D	"	"	D-1
"	E	"	"	E-1
"	F	"	"	F-1

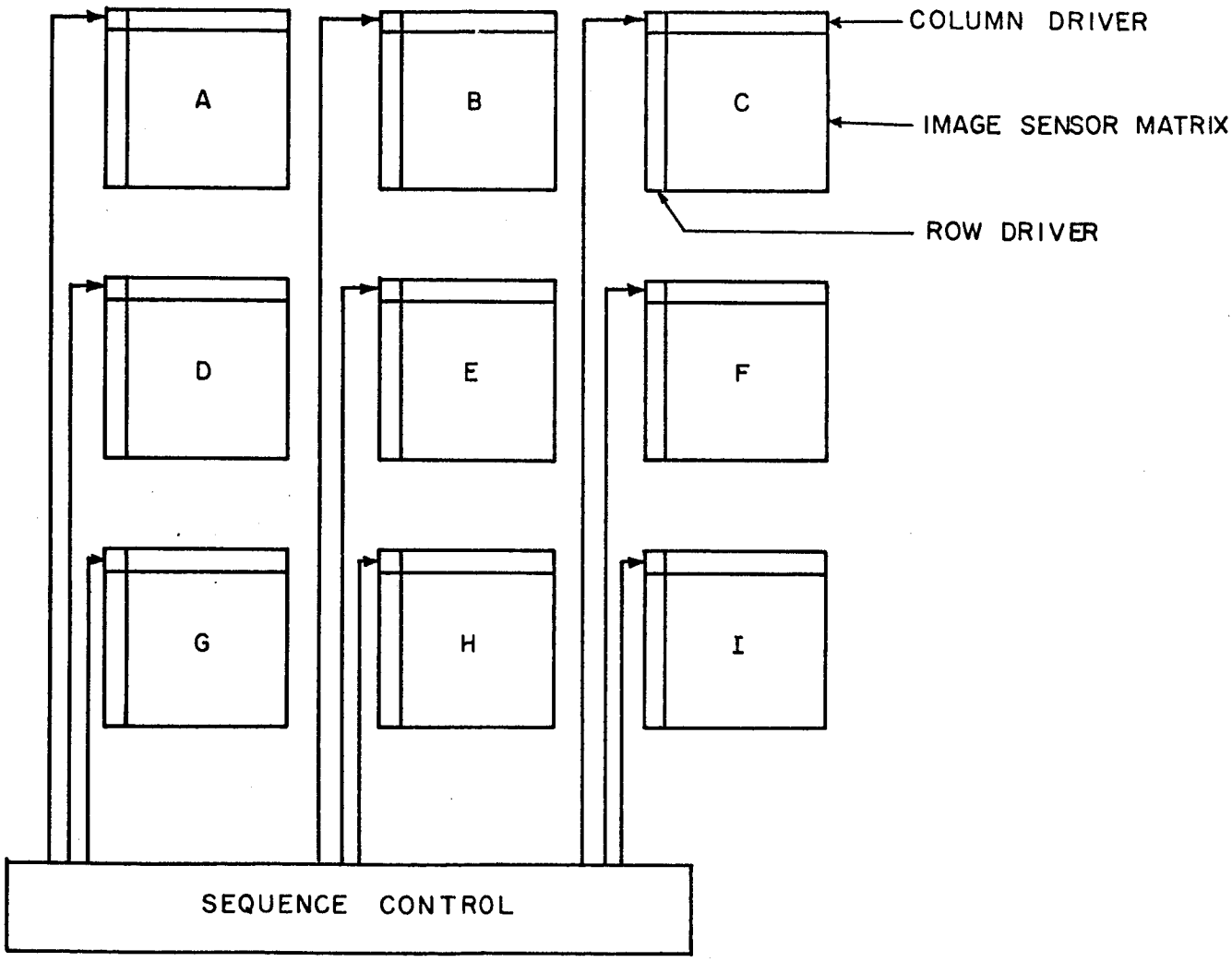


Figure 55

System Organization of Submatrices

pulse	D		scan row	D-m
"	E		" "	E-m
"	F		" "	F-m
"	G		" "	G-1
"	H		" "	H-1
"	I		" "	I-1
	.			
	.			
	.			
"	G		" "	G-m
"	H		" "	H-m
"	I		" "	I-m
"	A		" "	A-1
"	B		" "	B-1
"	C		" "	C-1

These submatrix elements can be closely packed to form a near continuous image sensor surface. If spacing were neglected, a grouping of 5 x 5 submatrices of size described in scheme II, would completely fulfill the program goals--600 lines, 300 lines/in, 2 x 2 in surface. Practically, however, some spacing must exist between the submatrices and the surface area would be slightly enlarged. A more serious problem, however, is the loss of the image in the spacing area. One solution is the use of a fiber optic bundle to bring the image to each submatrix individually, eliminating the image loss.

Another consideration is the fact that since the complete sensor must be subdivided, it is worthwhile to consider special applications where the partitioning can be put to advantage. A possible design, to illustrate the point, is a 360° image sensor. By arranging the submatrices on the periphery of a cylinder, and arranging individual lenses and aperture controls on an outer cylinder, a 360° view could be scanned and presented on a conventional TV display. A sketch of this design is shown in Figure 56 .

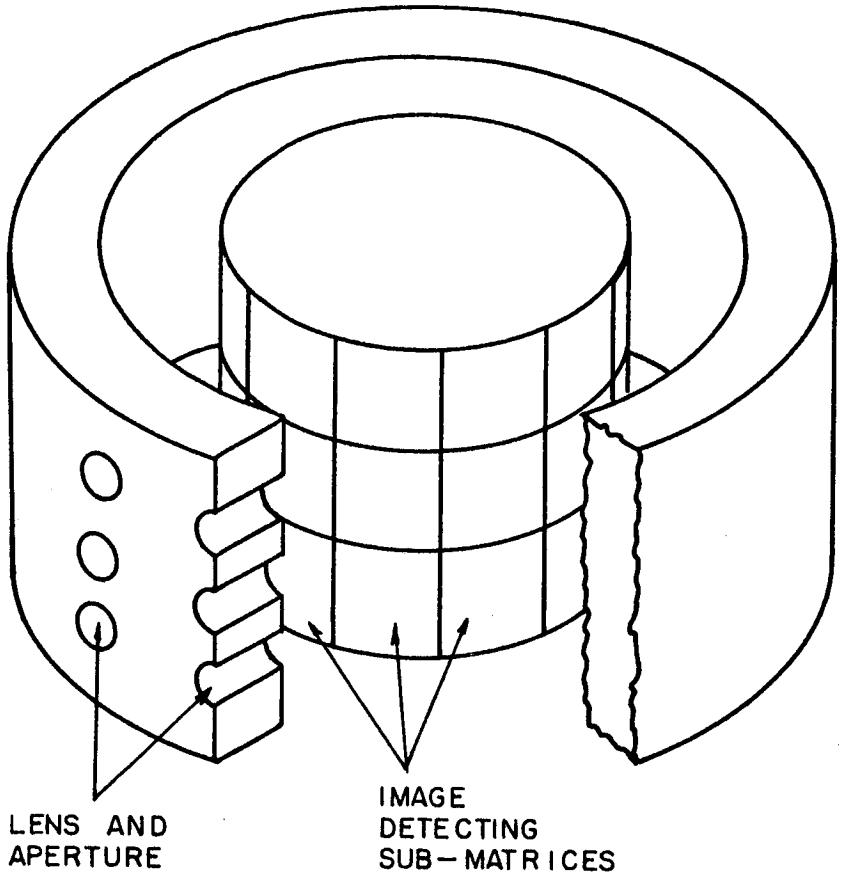


Figure 56

360°C Scanning Technique

We, therefore, conclude that although a solid state image converter by matrix array techniques does not appear to offer high resolution by the direct approach, proper system utilization of the realizable matrices will result in not only the equivalent of the conventional image detector, but additionally can provide many special designs not otherwise possible.

FINAL REPORT

MAY 1963

DESIGN AND DEVELOPMENT OF SOLID STATE IMAGE CONVERTER FOR SPACE VEHICLES

Electronics Laboratory
General Electric Company
Syracuse, New York

Authors: T. E. Bray
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Contract: NAS8-5116

Requisition: TP2-831714

PREPARED FOR

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NASA
HUNTSVILLE, ALABAMA

ABSTRACT

This report describes the work performed under contract no. NAS8-5116, by the General Electric Electronics Laboratory, Syracuse, New York during the period 1 July 1962 to 31 May 1963, for the George C. Marshall Space Flight Center, NASA, Huntsville, Alabama.

Both analytical and experimental approaches to determine the feasibility of constructing a solid state imaging device which approximates vidicon characteristics are reported. The work performed has been subdivided into four major areas;

1) Sonic delay line scanning
2) Nonlinear element requirements
3) Photoconductor materials requirement
4) Image converter configuration and experiments

The Appendices contain a theoretical analysis of 1) love wave propagation and 2) converter matrix equivalent circuits.

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OBJECTIVE OF CONTRACT

Current and projected needs of spacecraft instrumentation have led to the conclusion that a compact image converter of all solid state construction would be of use in experimental investigations of many types. Concurrently, solid state technology has progressed rapidly on many fronts during recent years. Hence, this project was concerned with determining the feasibility of constructing a solid state image converter comparable to a vidicon in operational characteristics. The image would be converted to a time sequential electrical output.

The scanning method to be used would be a set of acoustic stress waves, since the velocity of sonic propagation in solids is low enough to make relatively small converters potentially feasible. It is well known that scanning of a two dimensional image will result in undesired signals from unselected image elements unless precautions are taken. Hence, suitable nonlinear devices, as well as the photosensitive transducer were to be searched for.

MAJOR CONCLUSIONS

The results of experimental and analytical work performed during this contract indicates the feasibility of a solid state image converter with an electrical output and a slightly limited resolution. The tapped delay line converter configuration offers a workable solution to the interrogation problem superior to other methods studied. Available photoconductors and nonlinear diodes are suitable for operation of an image converter with a low resolution. Increased resolution requires changes in diode and photoconductor characteristics, which can be accomplished through increased materials development. The converter can be described by an equivalent circuit, and its requirements predicted for larger arrays of elements.

I. SCANNING TECHNIQUES AND MATERIALS

The following sections describe the work done on the problems associated with ultrasonic scanning techniques. Two essentially different areas of effort were involved and these will be described chronologically so as to point out the overall direction of this aspect of the program.

The first area of effort depended upon the use of an ultrasonic delay medium as a scanning mechanism only. If the imaging area is thought of as an array of individual photosensors, the delay line assembly merely serves to control the flow of electrical energy to a selected photosensor; it does not, however, need to serve as a source of electrical energy since a stress sensitive impedance change is sought. This approach to the problem was considered through the use of stress sensitive diodes which might react in a nonlinear manner to an acoustic stress propagating in a delay medium. In this way an acoustic pulse would be used to directly vary the impedance of a selected portion of the stress sensitive material, which would activate the corresponding photo-sensor in the imaging area. This approach appeared attractive from two standpoints: first, reliance was not placed upon an internally supplied voltage (from the scanning layer); and, second, a dc path for video current flow could be established.

For reasons to be described, this approach did not show sufficient promise to warrant further effort during this period, and the second area of effort was investigated throughout the remainder of this contract. The second method depends on the use of an ultrasonic delay line as both a scanning mechanism and an electrical voltage source capable of driving the associated circuitry. Due to the availability of highly active thin piezoelectric ceramic sheets, this method has demonstrated the most promise, was studied in some detail, and is now being actively pursued.

Stress Sensitive Diodes - A potentially useful scanning method can be based upon an effect recently described* in the literature. It has been found that shallow PN junctions may exhibit a stress sensitive re-

*Resistance of Elastically Deformed Shallow PN Junctions, W. Rinder, Journal of Applied Physics, Vol. 33, No. 8, August, 1962.

sistance and hence might be used in conjunction with a scanning stress wave to vary the resistance of a point in an imaging array. It was felt that this method warranted further investigation to determine the degree of nonlinearity* when a high frequency stress was applied to the diode.

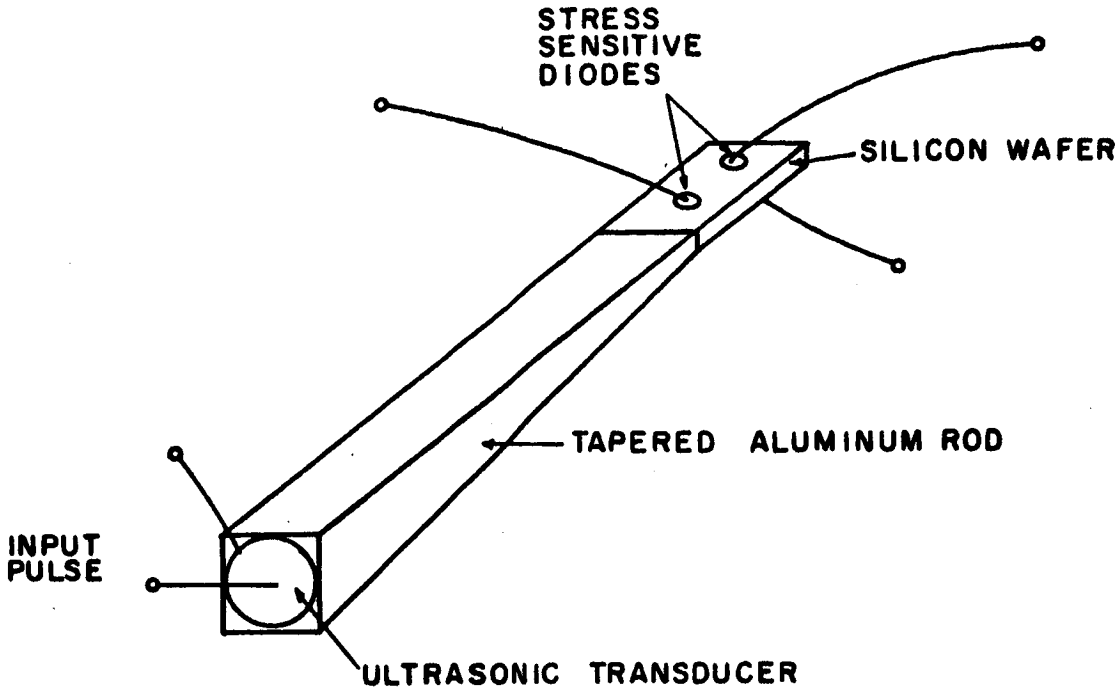
Several arrays of silicon planar diodes were fabricated from 0.9 ohm-cm, N-type silicon. The approximate size of the starting wafers was 0.010" x 0.25" by 0.5". The silicon wafers were first thermally oxidized, forming a silicon dioxide surface masking layer about 4000 Å thick, and holes were formed in the oxide. Boron was diffused to form the diodes, and the back was nickel plated after removing the oxide.

The diodes were subjected to stress in two ways. First, a diode array was bonded to a piezoelectric ceramic resonator as shown in Figure 1. The ceramic bar was side plated and driven in its longitudinal mode of vibration at a frequency of 46 kilocycles.** This scheme permits the generation of an alternating stress in the plane of the silicon wafer, the level of stress being proportional to the amount of 46 kilocycle drive supplied to the bar.

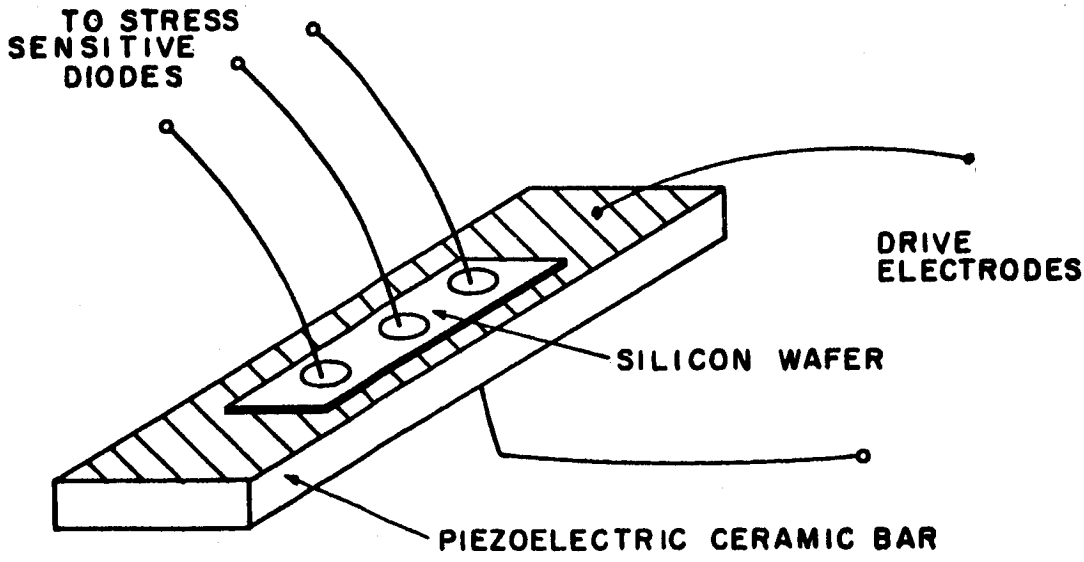
The second method of applying stress is shown in Figure 2. A silicon wafer was bonded to the end of a tapered aluminum ultrasonic delay line. This method permitted the generation of a high frequency acoustic pulse at the input transducer; the pulse traveled through the aluminum block and was coupled into the silicon wafer. Since the acoustic pulse travels through the silicon in the same manner as an acoustic scanning wave, this configuration is more consistant with the eventual application of the diodes than is the resonant ceramic bar.

*The need for nonlinearity is described in Section 2.

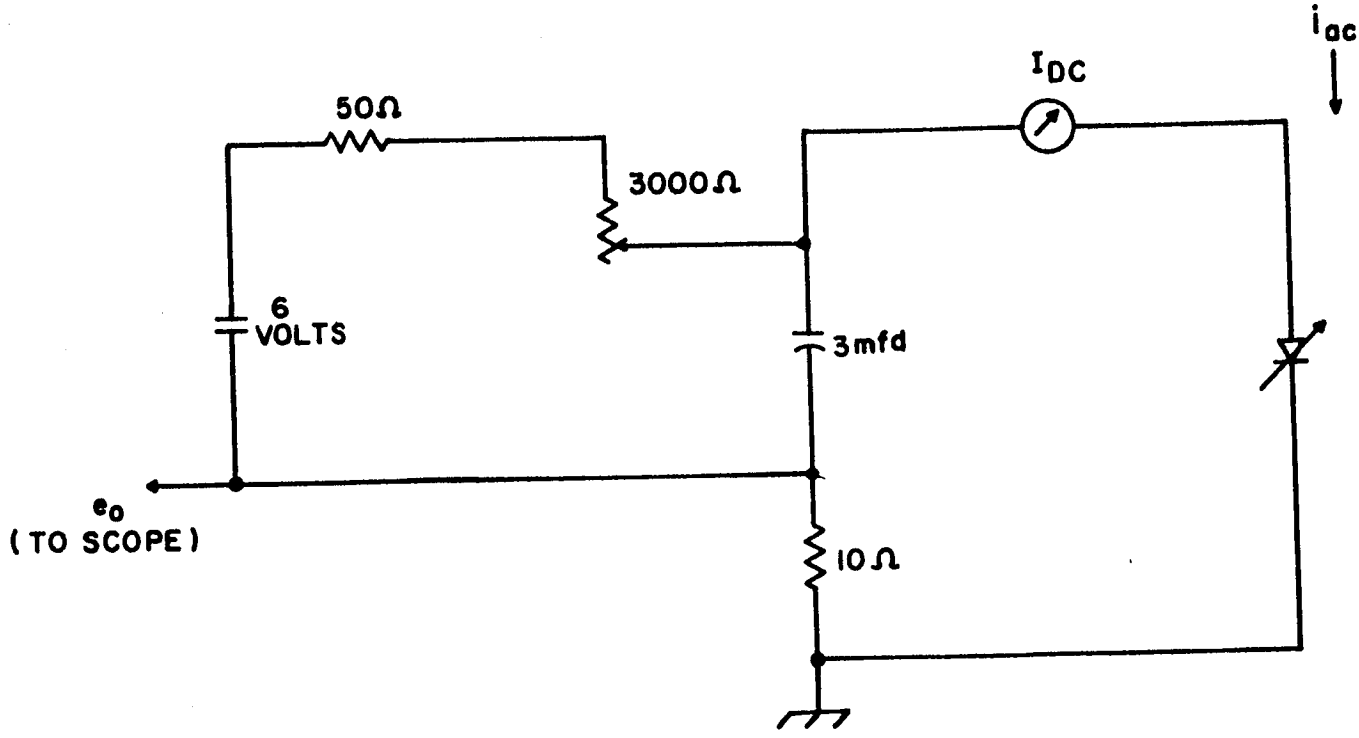
**Solid State Magnetic and Dielectric Devices, H. W. Katz, John Wiley and Sons, p. 105, 1959.



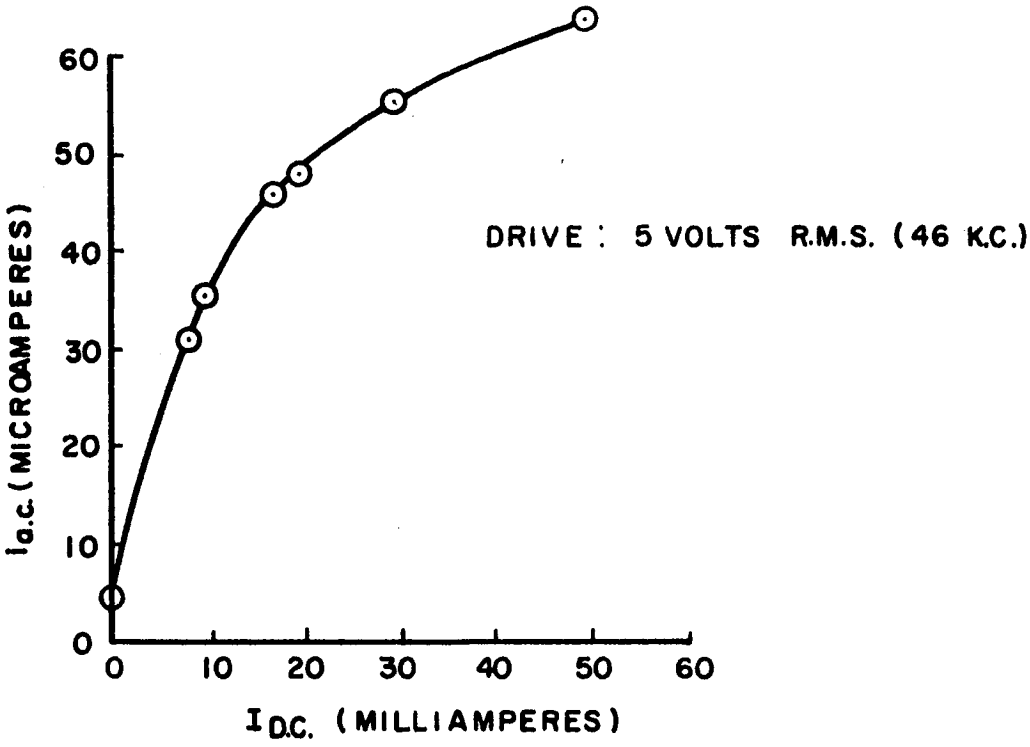
STRESS SENSITIVE DIODES ON
ULTRASONIC DELAY LINE
FIGURE 1

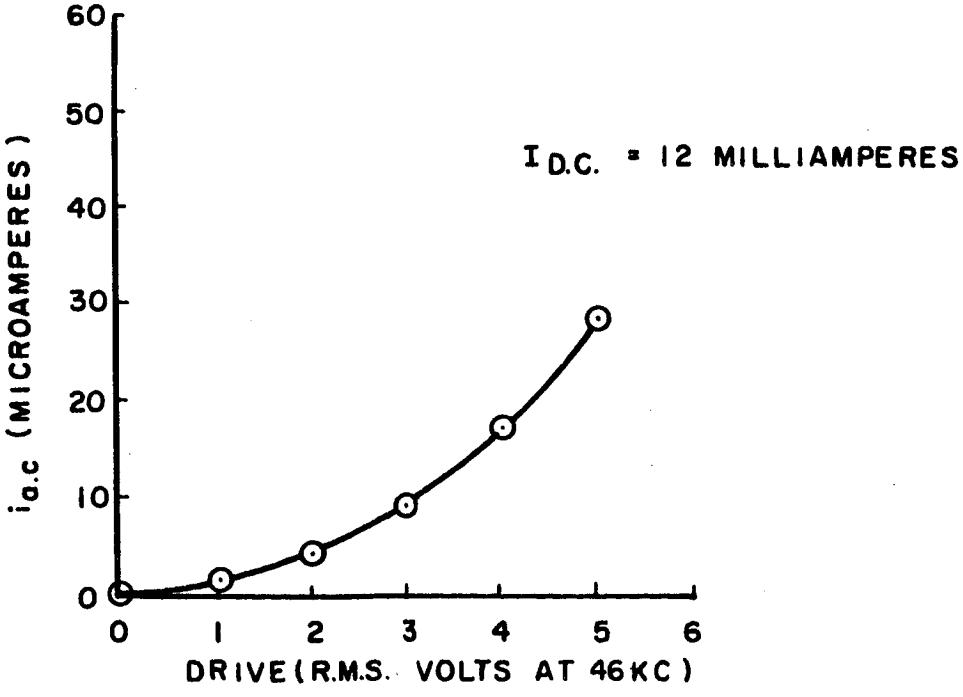


STRESS SENSITIVE DIODE ON
CERAMIC RESONATOR
FIGURE 2



DIODE TEST SET-UP
FIGURE 3





STRESS SENSITIVE DIODE CHARACTERISTICS
FIGURE 4

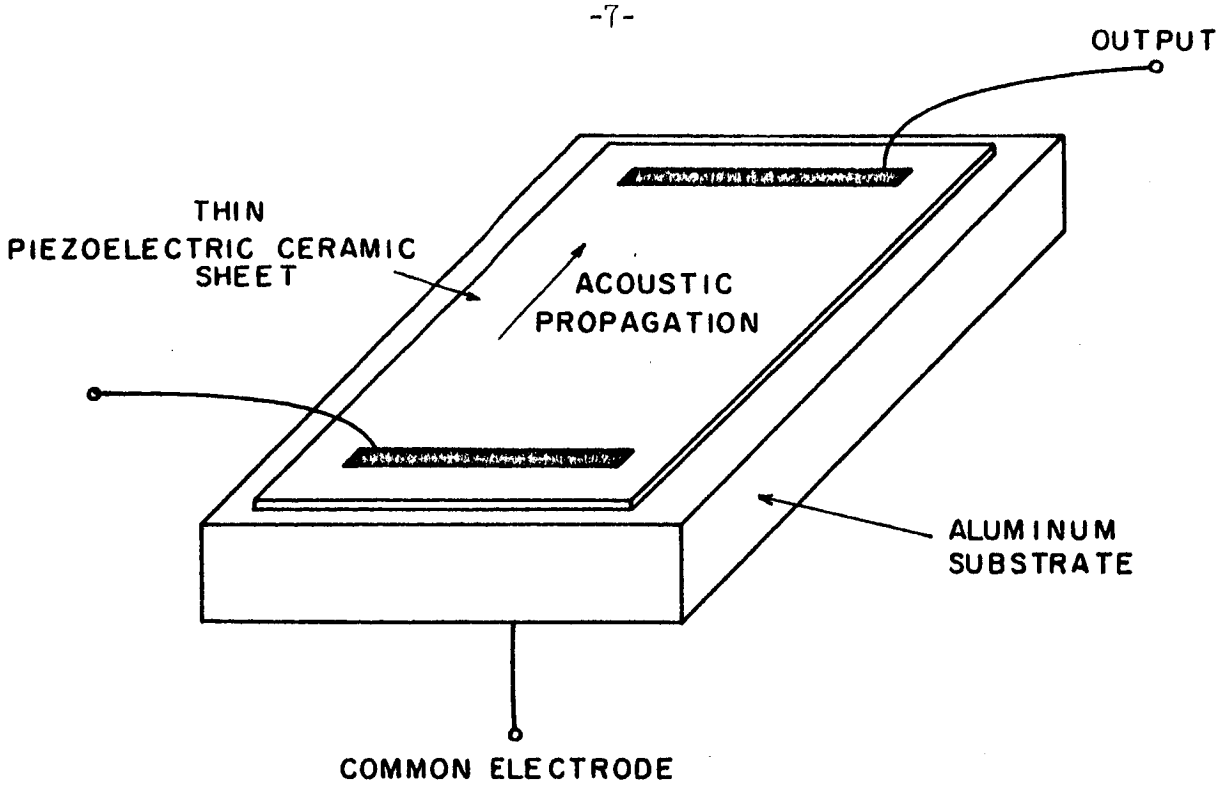
Figure 3 shows the test set-up used to evaluate the diodes. This circuit permits the observation of the ac voltage produced by the diodes under various conditions of forward and reverse bias voltages. Figure 4 indicates the results of the tests on the resonator configuration Although it appears that there is some nonlinearity between resistance and stress, it is much too small to be useful at present. Results of the delay line test were even less encouraging since no resistance variation was detected.

Because of these negative results, it was decided that further work on this approach be postponed and that emphasis be placed on the use of delay lines capable of supplying an electrical drive signal directly.

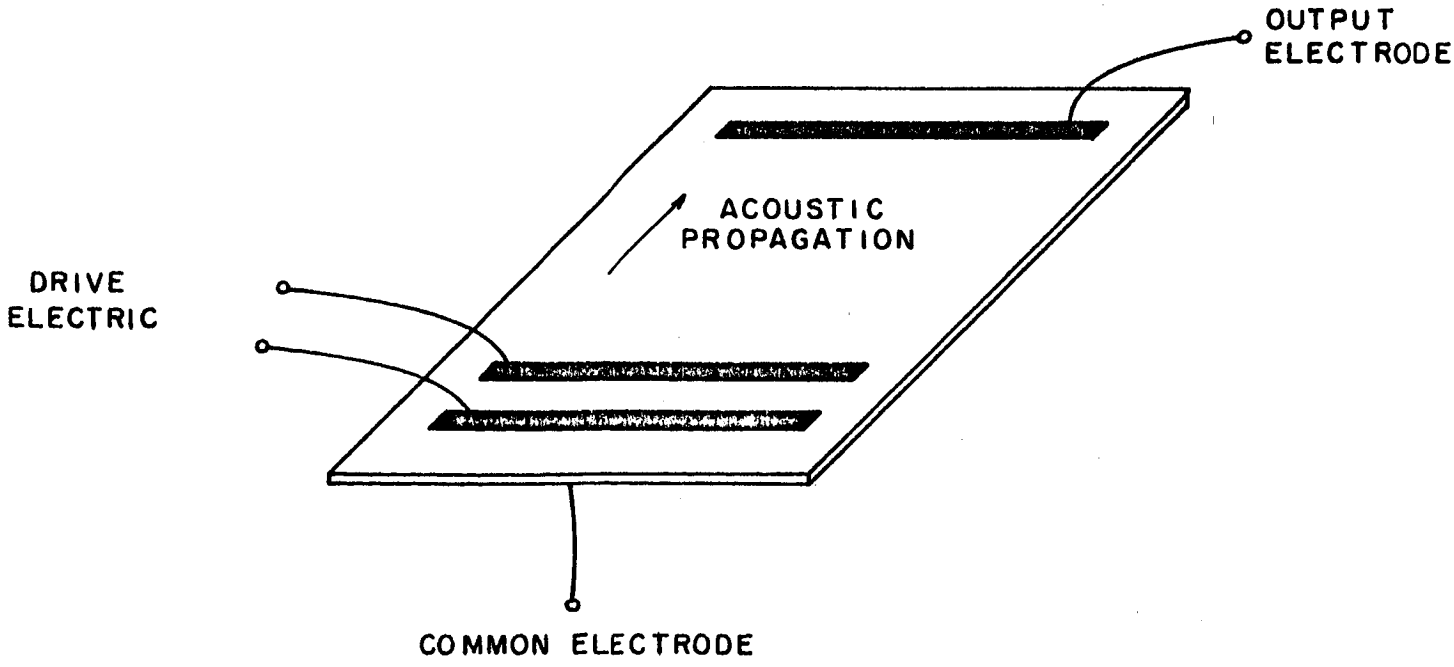
Thin Ceramic Sheet on Aluminum Substrate - A thin piezoelectric ceramic sheet may be used to form a high frequency ultrasonic delay line. One possible configuration is shown in Figure 5. A sheet of ceramic is polarized in its thickness direction and is bonded to an aluminum substrate with a conductive epoxy glue. The aluminum serves as a common electrode, and input and output electrodes are applied to the top surface of the ceramic. This configuration allows for the use of a very strong substrate to provide mechanical support for the ceramic delay sheet and to carry the majority of the acoustic energy in the scan wave.

Since the voltage at the output taps of this line would be used to drive a photosensor in the imaging array, the waveform observed at this tap should be free from extraneous pulses and reflections. In practice, however, it was found that severe waveform distortion was produced because of multiple acoustic reflections at the ceramic-aluminum interface. A theoretical analysis confirmed the observed fact that a thin layer media supported by a thick substrate will not, in general, provide propagation of an elastic stress wave, either shear or longitudinal, with good fidelity. This analysis is included in the Appendix of this report.

Thin Ceramic Sheet Delay Lines - A thin elastic sheet provides a good acoustic delay medium if the material has low acoustic loss and the sheet thickness is much less than an acoustic wavelength. If the sheet



CERAMIC DELAY LINE ON ALUMINUM SUBSTRATE
FIGURE 5



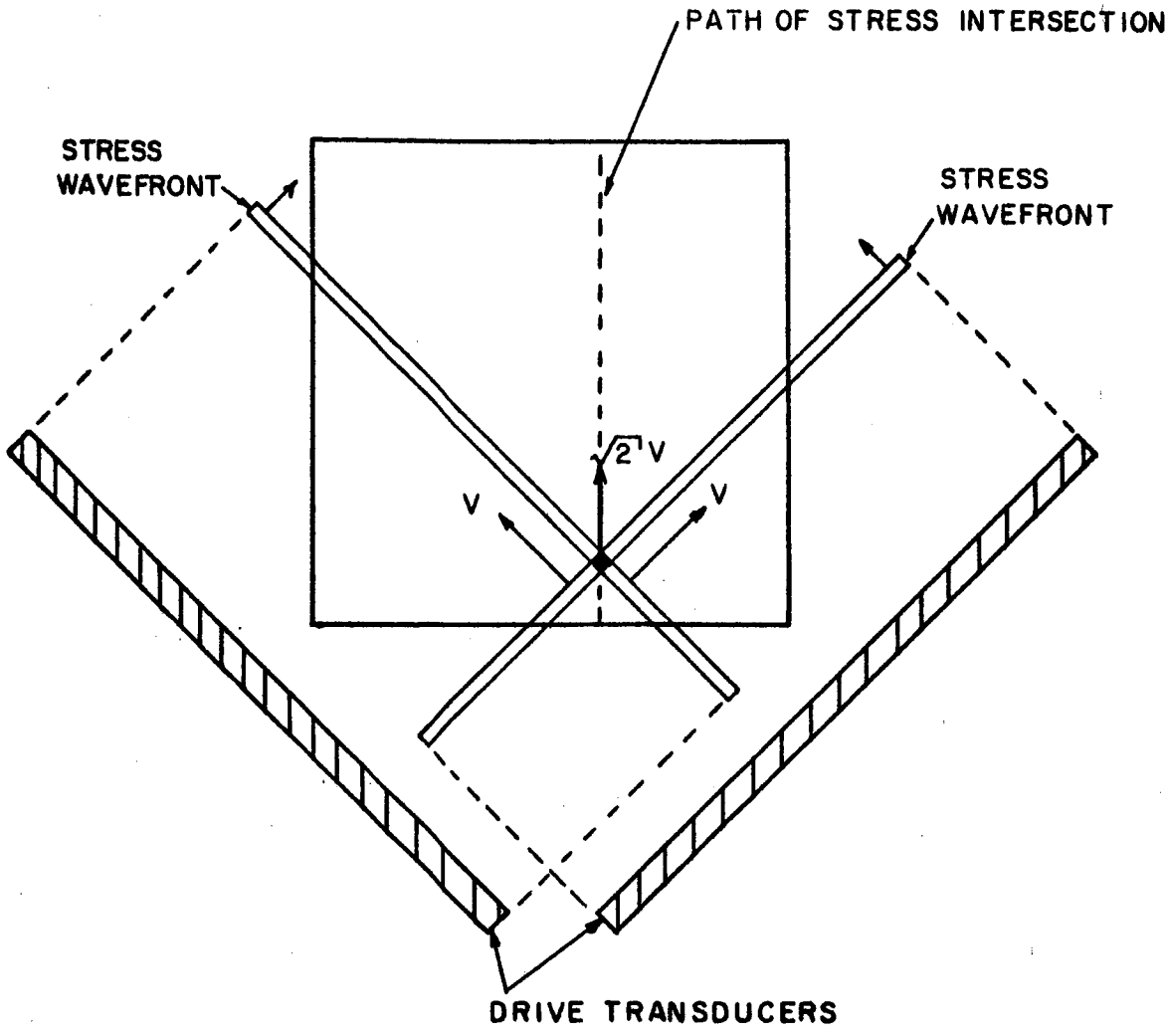
CERAMIC DELAY LINE
FIGURE 6

is a piezoelectric ceramic, a large number of electrodes can be placed along its length in order to provide multiple outputs or inputs. A thin piezoelectric ceramic sheet with two input electrodes and one output electrode is shown in Figure 6. Thin sheets of Gulton Lead Zirconate Titanate ceramic about 0.005" thick have been used successfully as active delay media at frequencies from 2 megacycles to 20 megacycles. At the present time, it appears that thin ceramic sheets provide the best available delay media. Delay sheets up to six inches long have produced outputs of several volts when the drive pulse was about one hundred volts.

The acoustic attenuation of this program has varied from 7 db/inch to 2 db/inch. Variations among seemingly identical sheets have been found. Acoustic reflections occur at every edge of the ceramic sheet. These reflections cause the propagation of several spurious pulses in the delay sheet. These reflections are reduced considerably at present, by covering the edges of the delay sheet with a soft asphalt acoustic absorber. Electrodes are presently applied by sputtered deposits of gold. These electrodes are sufficiently thin that they do not affect the propagation of the acoustic pulse as did earlier Ag paste electrodes. However, rather large anomalous fluctuations in the output voltages of various electrodes have been noticed. It appears that this may be due to variations in the quality of the gold electrodes.

Scanning Methods - When work was initiated on this program, the proposed method of scanning the image area consisted in using the point of intersection of two acoustic waves in a slab to produce either a double voltage or a double stress at a single point of the imaging area. This scheme is illustrated in Figure 7. The nonlinear and photoconductive layers lie directly on the scan media, and the scanning speed for an orthogonal scan geometry is $\sqrt{2}\,v$, where v is the velocity of sonic propagation in the delay material.

This method has the advantage that all the layers are in intimate contact so that interconnections are not required. This method does have several disadvantages, however. First, the spot formed by the inter-

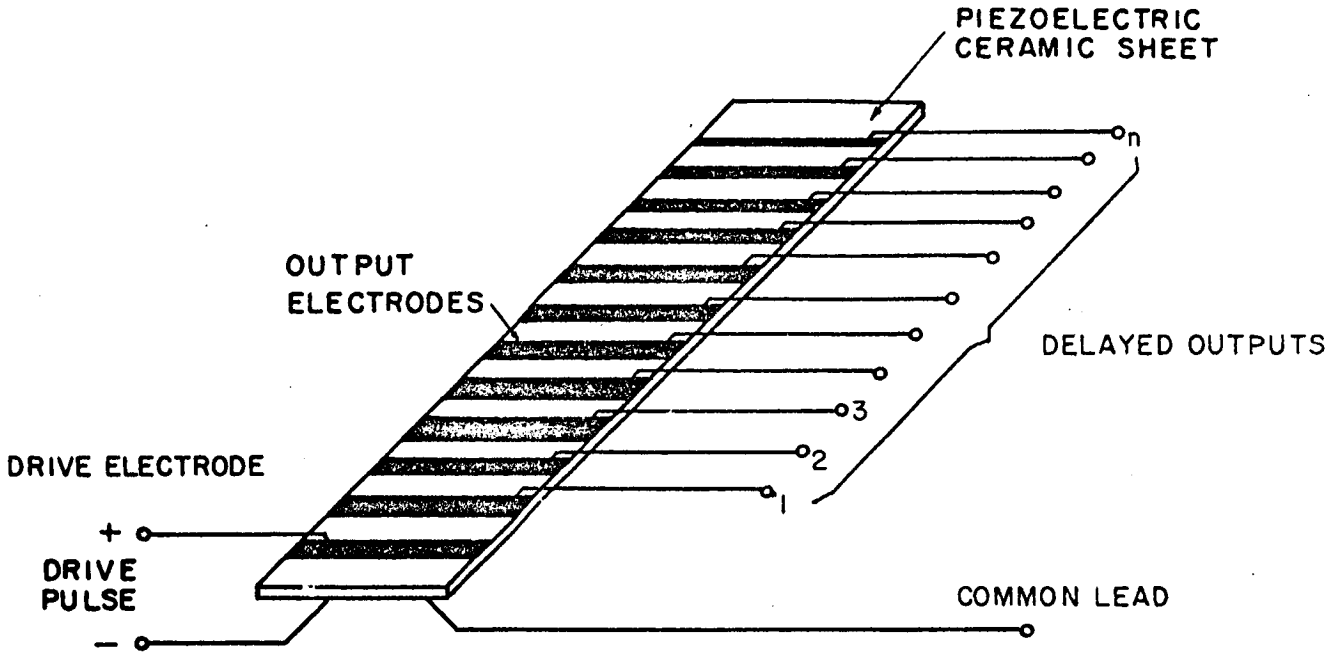


INTERSECTING SCAN METHOD
FIGURE 7

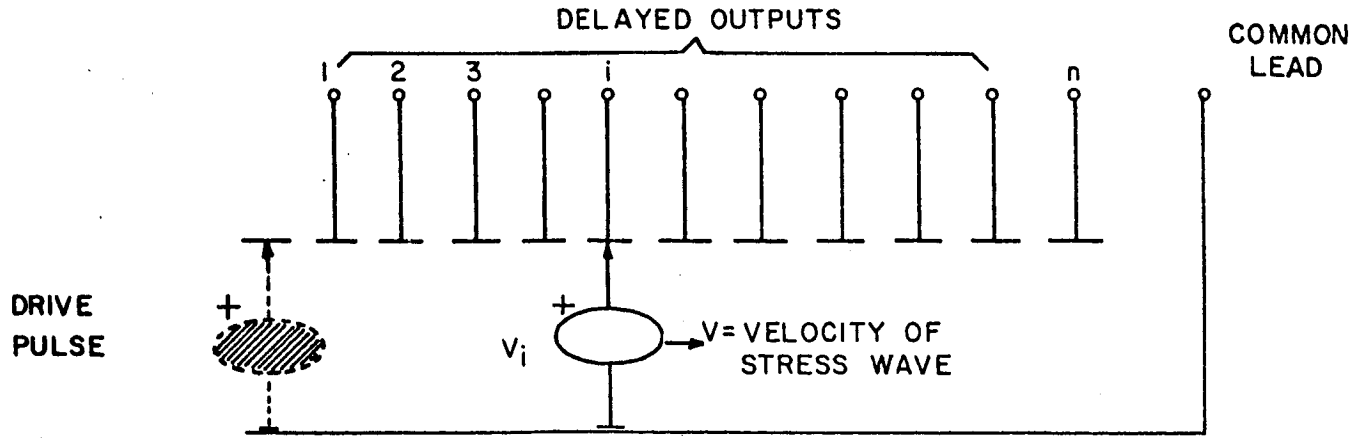
secting lines (assuming the sheet is piezoelectric) appears as a voltage source in series with a high capacitive impedance. This implies that photosensor load variations may adversely affect the double voltage scanning effect. A lower impedance source would be desirable. Second, the time required for the intersection to transverse the image area is determined by the image size and the sonic velocity of the delay material. A more flexible method allowing for slower sweep speeds would be desirable. Third, the effective size of the imaging area is considerably smaller than the necessary size of the screen due to the placement of the drive transducers. It would be desirable to use the available area more efficiently. Fourth, the optically active and nonlinear layers are in acoustic contact with the scanning layer, which would probably lead to acoustic interaction effects. Fifth, the electrical capacity of the output electrodes is known to reduce the available output signal voltage, and finally, it would be desirable to compensate the change of scan voltage with distance which will occur in the piezoelectric slab.

These factors suggest that another scanning method be considered. This method employs two physically separate thin sheet delay lines, as illustrated in Figure 8a, to simulate the intersecting scan. Each delay line has multiple output taps, as shown, and operates electrically much as a "traveling" pulse voltage source, with an equivalent circuit like Figure 8b. A conductor matrix connected to all output taps and incorporating a photoconductor and nonlinear element at each conductor intersection, forms the image plane, as shown in Figure 9. The video signal is developed across the load resistor shown, which completes the series current path between the two delay lines.

The desired electrical operation may be represented at one particular instant in time by the simplified circuit in Figure 10, if the adverse effects of the rest of the matrix are temporarily ignored. The voltage sources represent the pulse outputs of particular delay line taps. If these pulses occur at different times, very little current will flow through R_L, since a single pulse voltage is not sufficient to turn on the diode. If, however, these pulses occur together, almost twice the



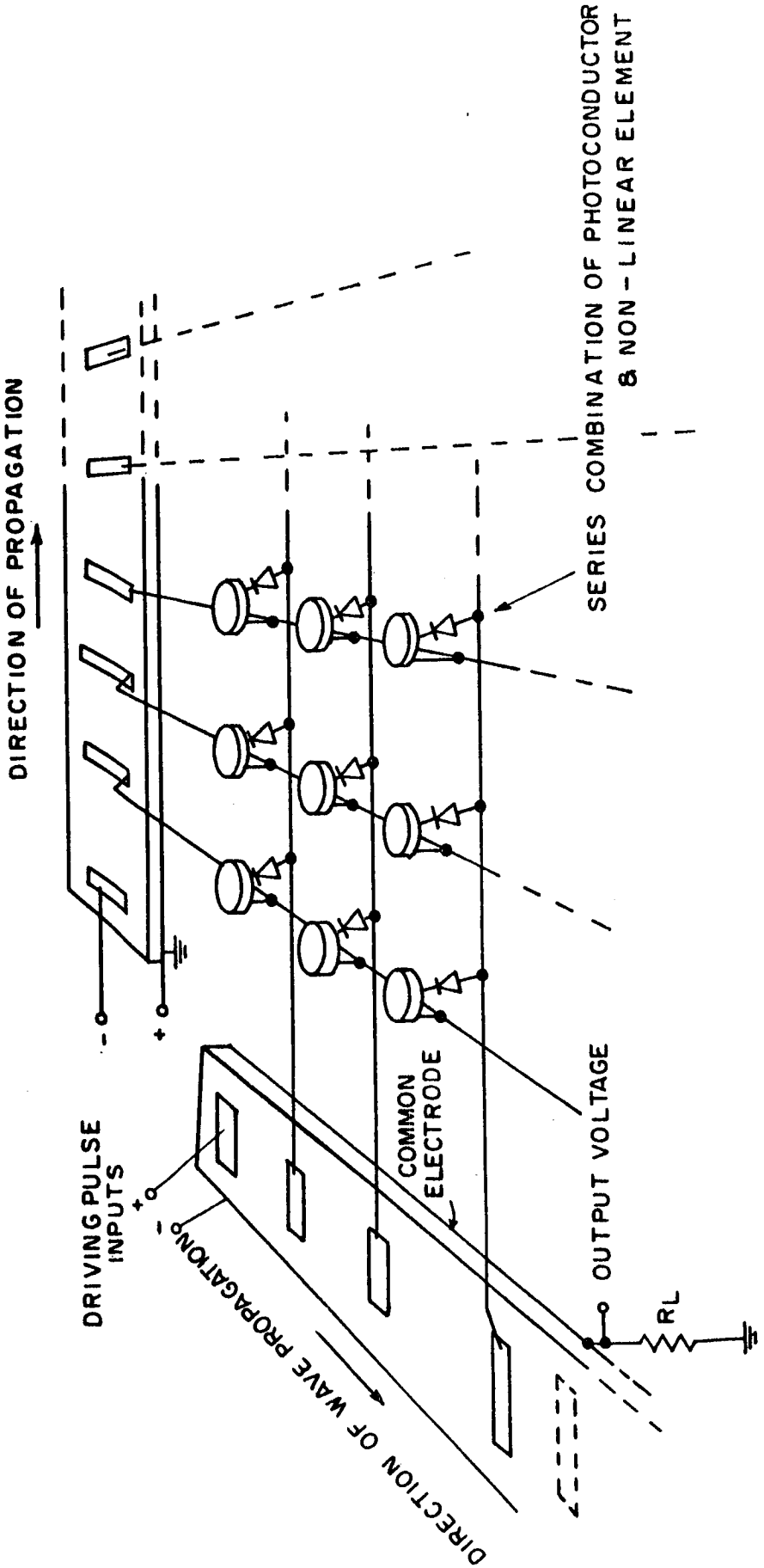
a) PICTORIAL REPRESENTATION



b.) EQUIVALENT CIRCUIT

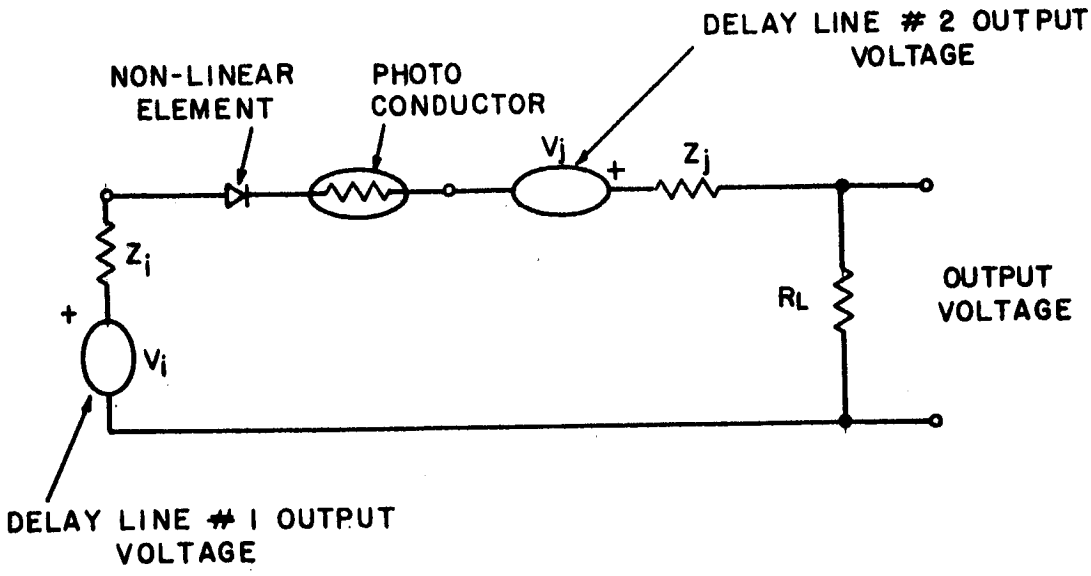
MULTIPLE OUTPUT STRIP DELAY LINE

FIGURE 8



GENERAL FORM OF THE IMAGE CONVERTER (9 ELEMENTS SHOWN)

FIGURE 9



SINGLE ELEMENT EQUIVALENT CIRCUIT

FIGURE 10

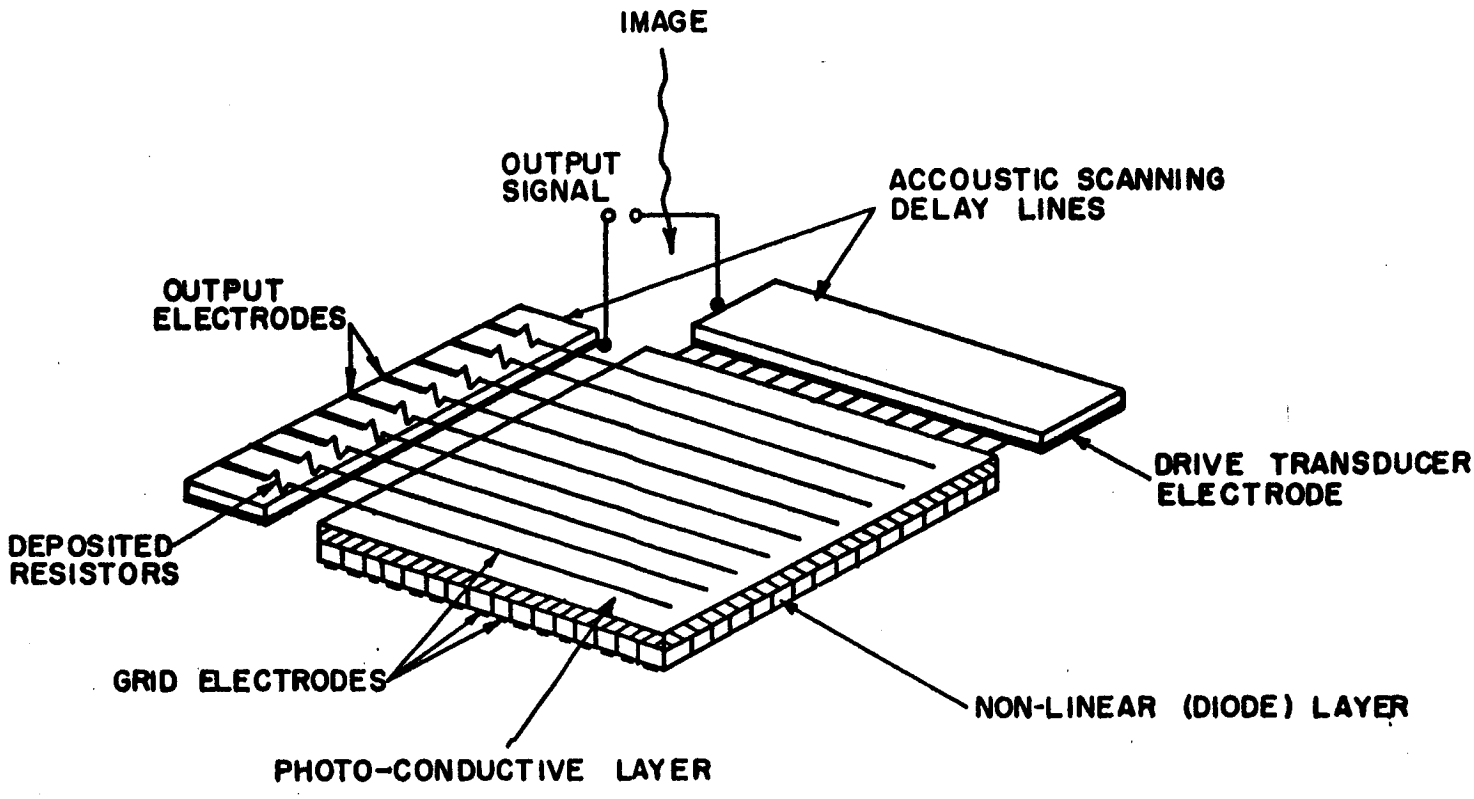
previous voltage appears across the diode and a much larger current flows. In this case, the photoconductor is the dominating resistance in the circuit, so that its changes are reflected in the current variations through the common load resistor, and the incident light on the photoconductor is determined.

It is immediately apparent that this configuration alleviates the first disadvantage of the intersecting scan method; the large output electrodes imply that the electrical source impedance of the tap will be relatively low. The delay line output voltage will, therefore, be less affected by load variations in the photosensor circuitry.

The third disadvantage of the intersecting scan method can be overcome by placing the separate delay lines behind the imaging area since only electrical connections to the imaging area are required. For the same reason, the delay line lengths may be adjusted to control the sweep speed.

This emphasis on discrete elements also simplifies the analytical treatment of the image converter operation. Interrogation of an element can now be considered in two parts. The first consideration is that of the photoconductor current flowing directly through the load, as shown in Figure 10. The second consideration involves the shunting paths provided unavoidably by the other matrix intersections, and the passive delay line taps. This shunting effect places further constraints on the converter elements, which become practically more severe, as the number of elements is increased, as will be seen later.

The equivalent circuit approach, then, will aid in determining these elemental operating characteristics, as a function of the number of elements, or equivalently, as a function of the resolution. These results can then be extended to determine the operations of an image converter consisting of photoconductive and nonlinear layers, where the preferred conduction is normal to the layers and the resolution is a function of the matrix conductor spacing, as illustrated in Figure 11.



VIEW OF PLANNED CONSTRUCTION
FIGURE 11

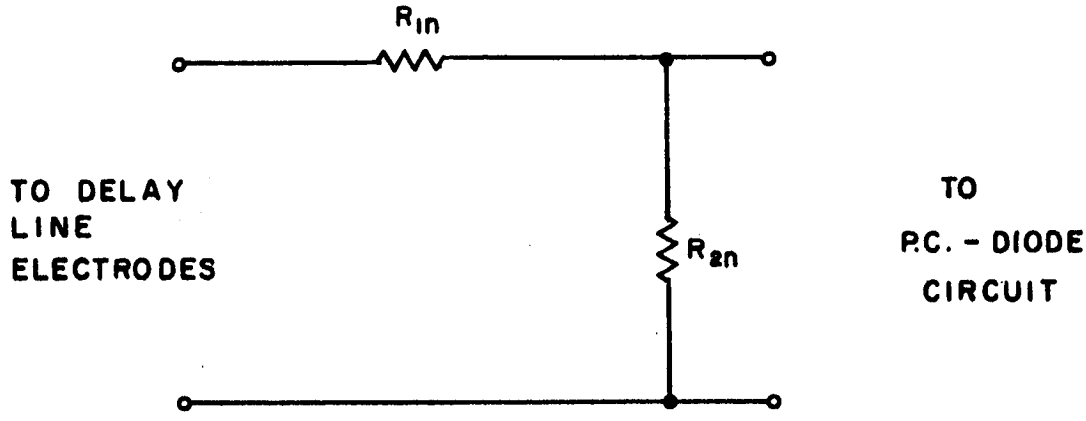
Capacitance calculations indicated the superiority of the "line" scan over the "slab" scan. Removal of the acoustic loading or interaction is evident. The supplying of a constant, low impedance voltage source may be accomplished via deposited resistor pads at each tap.

Delay Line Output Voltage - An acoustic wave traveling along a delay line is attenuated for several reasons. First, mechanical losses in the form of heating occur in any delay material. These losses are a property of the delay material and are inversely related to the mechanical quality factor, Q_m, of the material. At high frequencies, grain boundary scattering effects may also be included in this loss. A second source of attenuation is due to the energy extracted from the acoustic wave at each output electrode to drive the photosensor.

The construction of a photosensor array will be simplified if the output voltage from all the taps of the delay lines are equal. For this reason, the problem of providing a constant output voltage was studied during this period. At present, the method consists of placing a constant impedance output pad in each output electrode connection. It is anticipated that pads shown in Figure 12 will be used, since they may be deposited using currently available thin film techniques at the same time as the electrical connections to the imaging array are made.

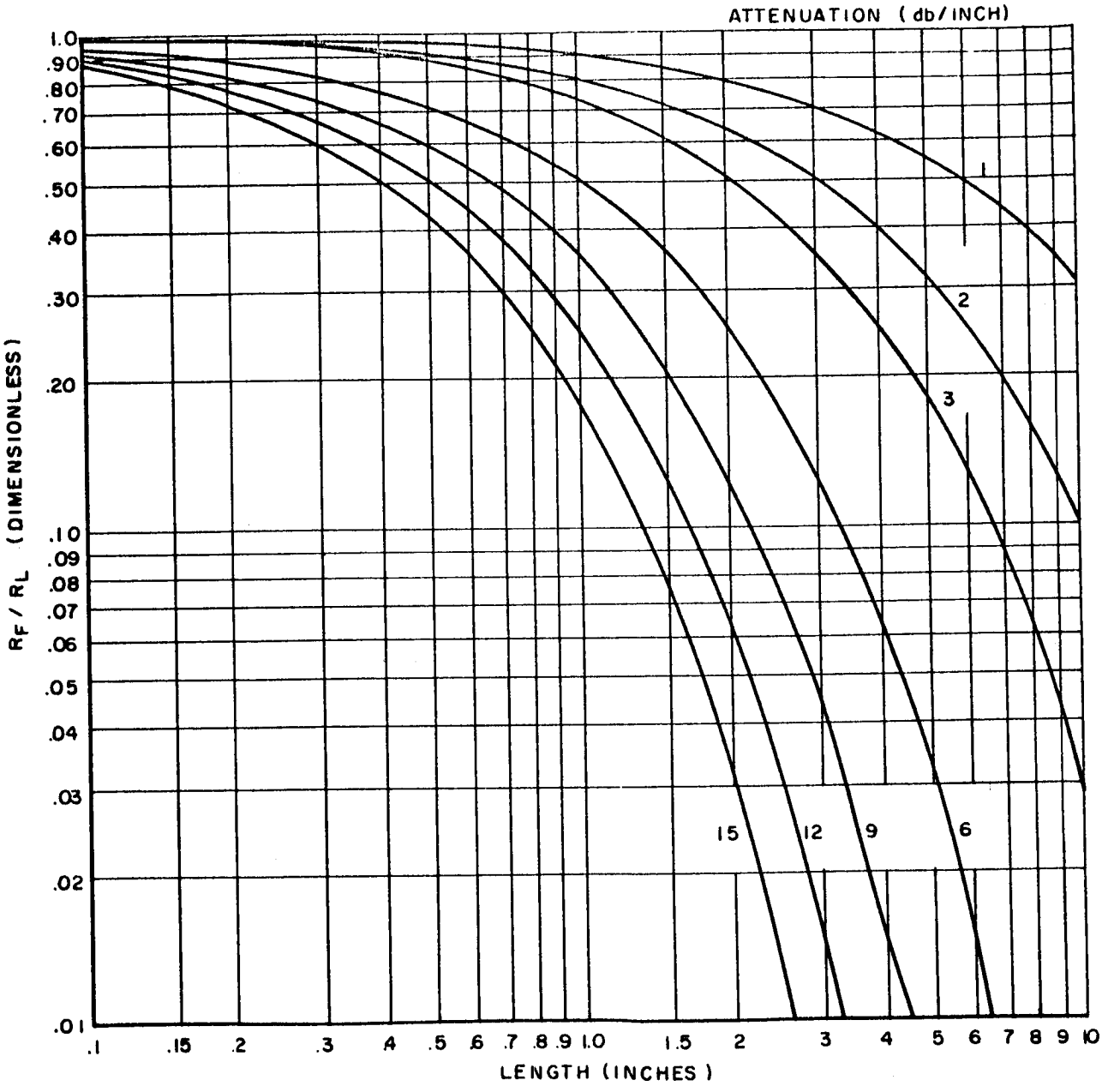
Figure 13 indicates the theoretical variation of the resistance R_2 as a function of delay line length and acoustic loss. This loss includes both the previously described causes. The calculations for Figure 13 were based upon the assumptions that the load on the delay line was constant (i.e., $R_1 + R_2 = \text{Constant}$) and that the photosensor circuitry load on the pad was negligible. The implication of these assumptions is that the largest value of R_2, normally on the last output, should be much smaller than the lowest photosensor impedance. Figure 13 then indicates the variation of R_2 at various taps along the delay line. R_1 should be chosen so that $R_1 + R_2$ is constant at each tap.

Tapped Line Fabrication - Two ten tap strip delay lines were in the configuration of Figure 8a, constructed from 0.005 inch Gulton sheet ceramic.



CONSTANT OUTPUT PAD

FIGURE 12



CONSTANT OUTPUT PAD RESISTANCE DISTRIBUTION

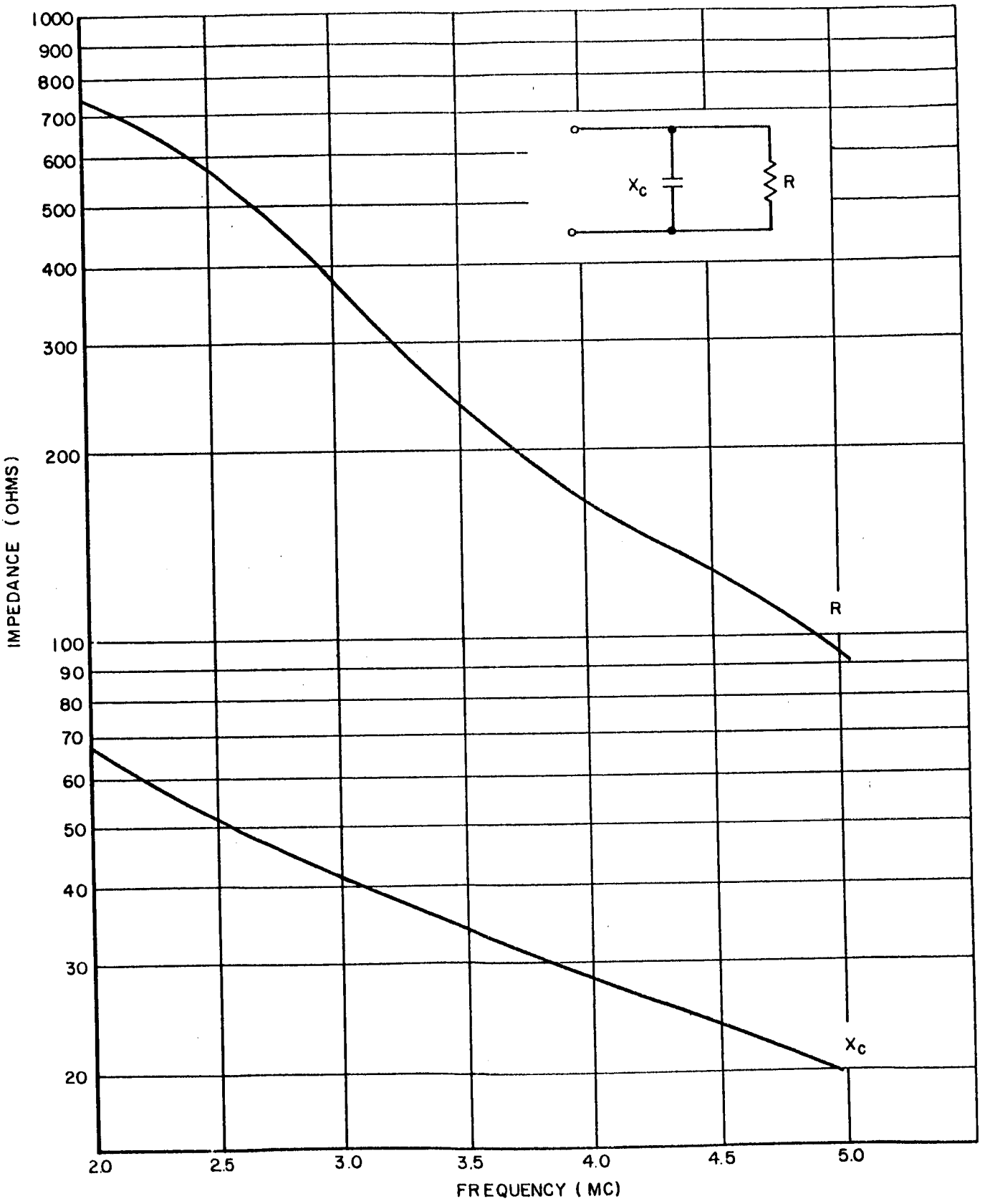
FIGURE 13

These lines were approximately 6 inches long and 0.5 inches wide. Each electrode was about 0.040 inches wide and consisted of gold sputtered on a thin layer of nichrome previously evaporated on the ceramic. The input impedance of a single tap is shown in Figure 14. Although these lines were successfully used for scanning in tests described in the following sections, the voltages obtained varied erratically from tap to tap. It was felt that this was due to variations in the gold electrodes. These electrodes were quite delicate and mechanically weak. It was decided to use a different electroding technique on the next lines constructed in order to overcome these objections.

The modified electroding procedure was applied to the construction of two fifty-tap delay lines. These lines were also approximately 6 inches long, 0.5 inches wide, and 0.005 inches thick. The electrodes were applied in three steps. First, a thin layer of nichrome was sputtered on for about 10 minutes in order to provide good adhesion. Second, a thin layer of gold was sputtered on for 10 minutes in order to provide a conductive substrate for the next step. Third, the electrodes were applied by electroplating a copper layer 0.0001 inch thick on the gold layer.

There was insufficient time to evaluate the electrical performance of these lines; however, the mechanical strength of the electrodes was much better than that of previous attempts. Leads were readily soldered to the copper electrodes, whereas this operation was extremely difficult with gold electrodes.

Several attempts to fabricate a shear mode delay line during the latter portions of this program proved unsuccessful. In order to maintain the desirable low impedance characteristics of the present electroding configuration, the polarization of a shear line must lie in the plane of the ceramic sheet and in the direction of its width. The high polarization fields have fractured all the sheets of 0.005 inch ceramic used to date. It is thought, however, that thicker ceramic sheets will withstand the polarizing field and will provide a useful delay medium for shear waves.



10 TAP DELAY LINE IMPEDANCE CHARACTERISTICS
FIGURE 14

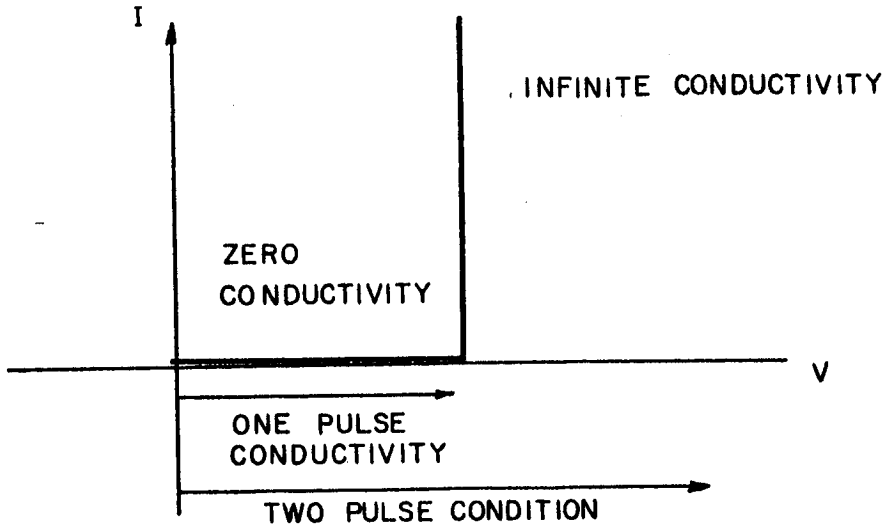
II. NONLINEAR ELEMENTS AND THEIR CHARACTERISTICS

The success of the image converter described in Section I depends upon the efficiency of the nonlinear elements used. It is essential that the signal current flowing through the load at any instant be a function of one matrix intersection only, the intersection with twice the pulse voltage across it. This requires that all other matrix intersections have a high resistance, even though they may have one pulse voltage across them. The ideal nonlinear element, then, would have a characteristic as illustrated in Figure 15a.

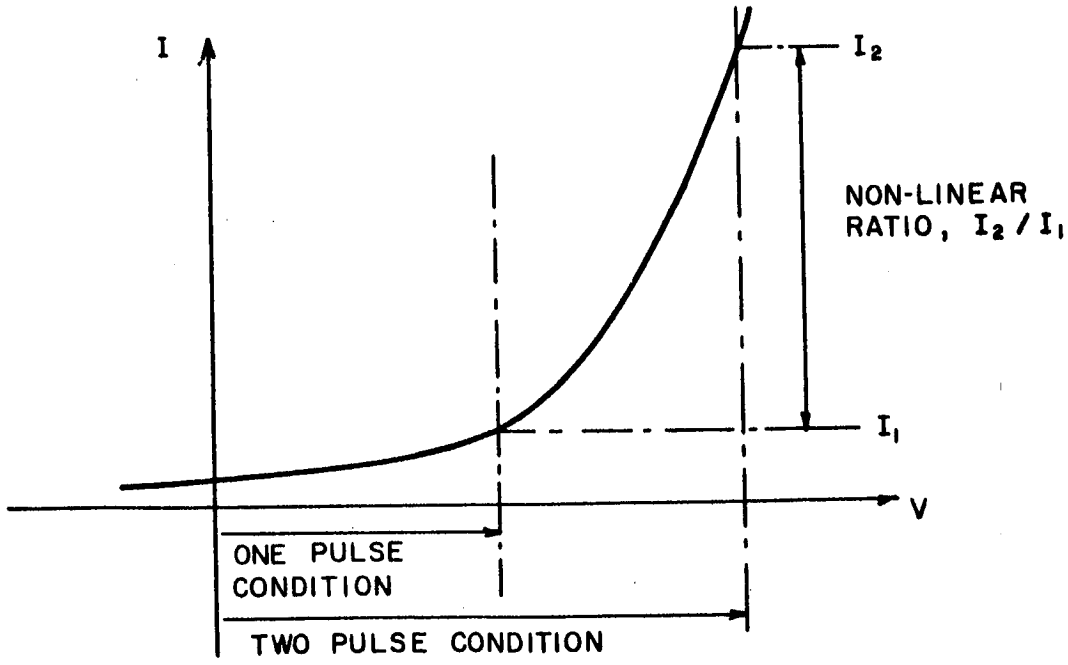
The simplest approximation of this ideal characteristic is the diode characteristic, shown in Figure 15b. With this element, there will be a small conduction with one pulse voltage and a large conduction with two pulses present. The ratio between these two values of conduction becomes a measure of the number of elements that can be incorporated and, therefore, of the ultimate resolution of the image converter. This nonlinear ratio must be several orders of magnitude to be effective.

In addition to obtaining a high nonlinear ratio, the "on" resistance must be low compared to the range of photoconductor resistance values expected, such that the latter represents the dominant parameter upon interrogation.

The nonlinear characteristics of a passivated silicon diode were studied, since Si is a wider bandgap material (and thus should be more nonlinear), and passivation reduces shunting effects. In particular, a General Electric SSD 558 Diode (planar epitaxial passivated silicon) was measured, since it was being used in conjunction with thin sheet delay lines. The measured characteristics of this diode are shown in Figure 16. The characteristics are seen to be exponential over a range of seven orders of magnitude. The data in Figure 16 has been used to obtain Figure 17 where the output voltage characteristics of a diode-resistor combination are shown as a function of input voltage from the delay line. Figure 18 indicates the nonlinearity ratio of the diode-resistor combination as a function of the half-voltage output of the delay line. The non-



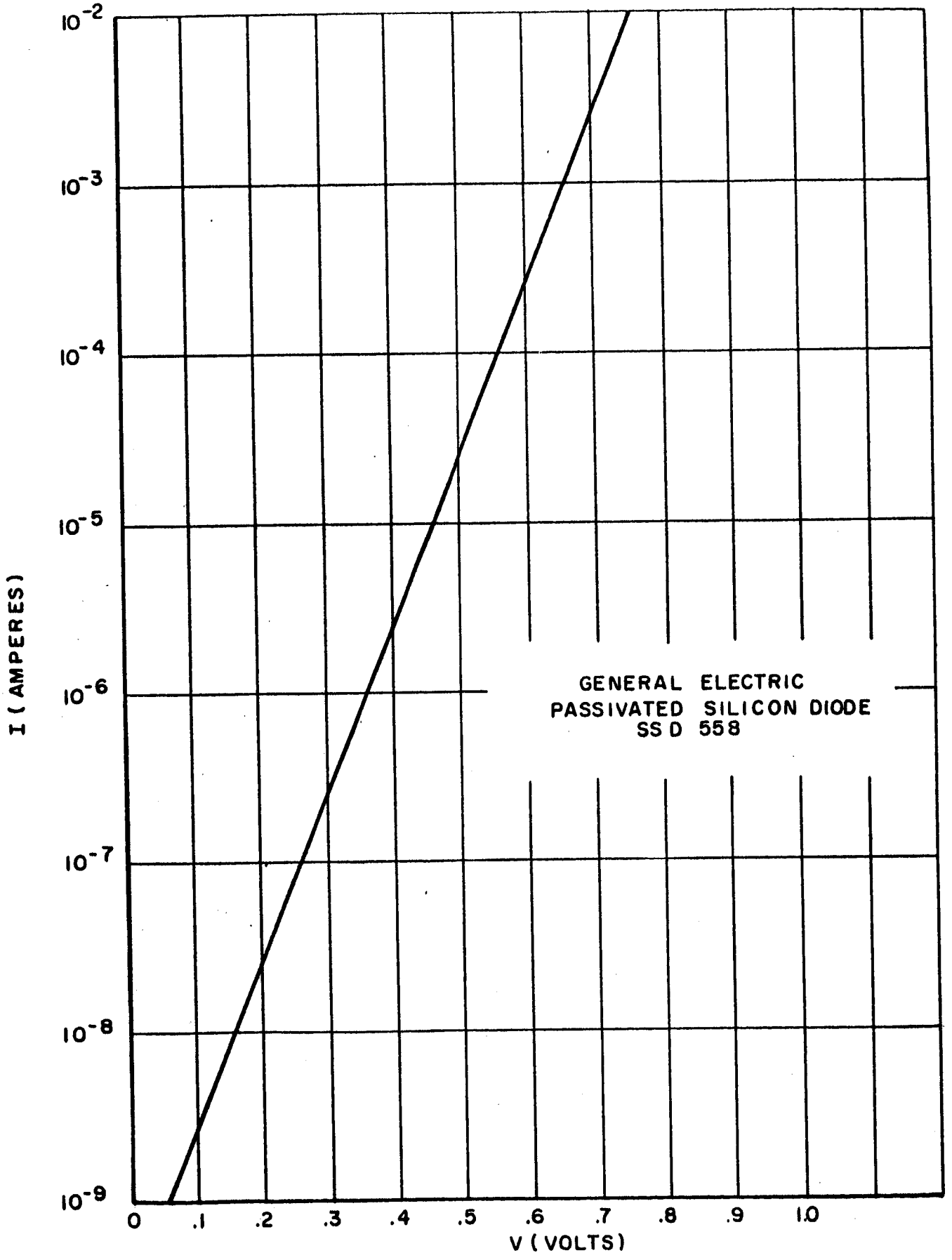
a.) IDEAL DEVICE CHARACTERISTIC.



b.) TYPICAL DIODE CHARACTERISTICS.

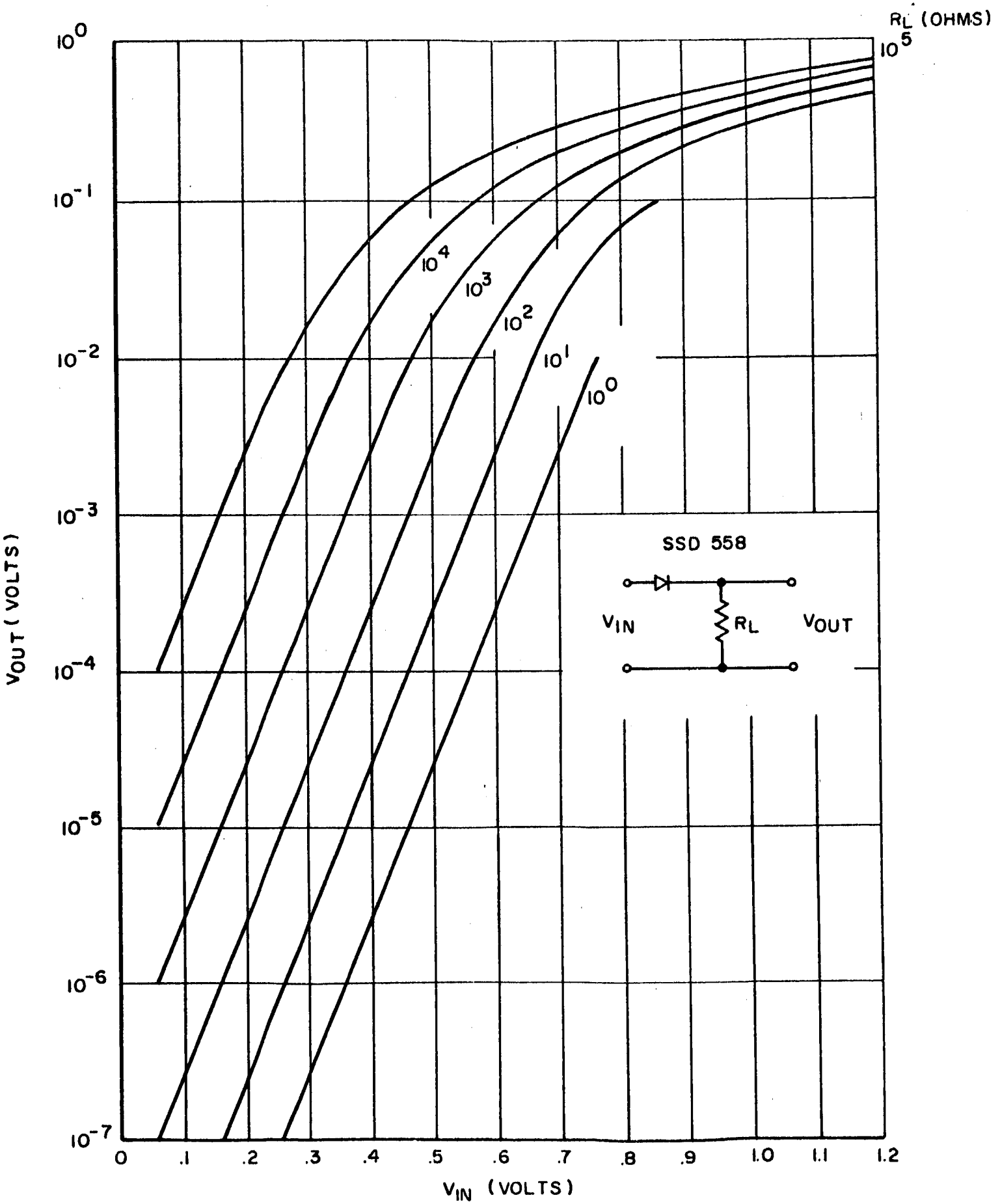
NON LINEAR ELEMENT CHARACTERISTICS

FIGURE 15



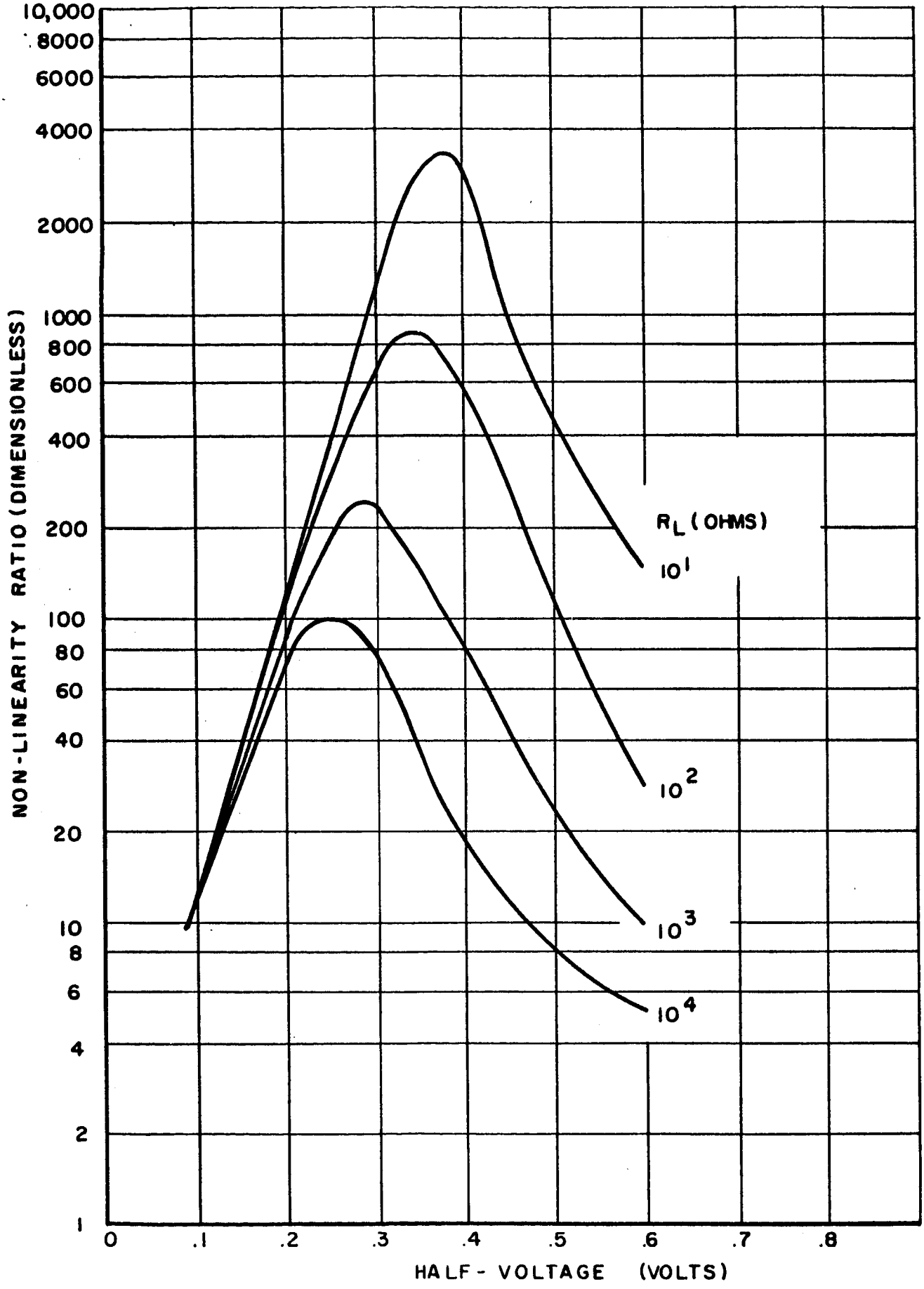
V-I CHARACTERISTICS OF SSD 558 DIODES

FIGURE 16



VOLTAGE NON-LINEARITY FOR SSD 558 DIODE

FIGURE 17



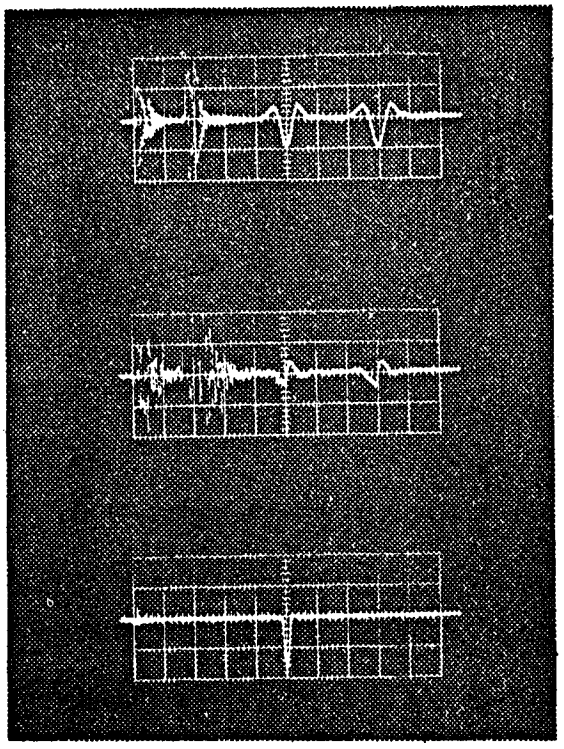
NON-LINEARITY RATIO FOR SSD 558 DIODE
FIGURE 18

linearity ratio is defined as the ratio of the output voltage with twice the half-voltage to the output voltage with only the half-voltage applied. Although rather high ratios are apparently possible, they have not been observed because of the loading effects of small values of R_L on the delay line and because the half-voltage output of the diode-resistor is too small to detect with video amplifiers. This point may be verified from Figure 17 where it is seen that much of the nonlinear behavior occurs at less than one millivolt levels.

Figure 19 shows the behavior of a diode-resistor combination driven by a sheet delay line. In these pictures R_L = 110 ohms and the delay line output was shunted by a resistance of 40 ohms. The top trace shows the input pulses to the diode-resistor. These pulses are staggered to simulate a half-voltage condition. The middle trace shows the voltage output in this condition. The bottom trace shows the voltage output when the half-voltages are made coincident. This condition corresponds to the interrogation of the combination. Figure 19 thus serves to verify the nonlinear output characteristics of the delay line, diode-resistor combination.

Because the pulse widths utilized in the image converter are less than a microsecond, the capacitance of the diode becomes an important factor. Even though the junction capacitance of a diode is essentially constant, at low levels of forward conduction, it can be large enough to represent a shunt across the high resistive component and seriously degrade the nonlinear action. At higher levels of forward conduction, however, the junction capacitance increases exponentially; if effectively utilized, this capacitance will contribute to proper switching action.

The capacitance of the SSB558 was measured on a Boonton capacitance bridge with an adjustable excitation voltage capable of measurements at one megacycle. This measuring technique closely approximates the actual operation of the element in the image converter, and allows a more direct utilization of the capacitance readings. The SSD558 capacitance was essentially constant at 2.7 picofarads, at low conductance values, and



TOP:
ELECTRODE PULSES (STAGGERED)
VERTICAL : 0.5 VOLTS / DIV.
HORIZONTAL : 0.5 μSEC / DIV.

MIDDLE:
OUTPUT PULSES (STAGGERED)
VERTICAL : 5 MILLIVOLTS / DIV.
HORIZONTAL : 0.5 μSEC / DIV.

BOTTOM:
OUTPUT PULSE (COINCIDENT)
VERTICAL: 0.1 VOLTS / DIV.
HORIZONTAL: 0.5 μSEC / DIV.

DIODE OUTPUT NON- LINEARITY
FIGURE 19

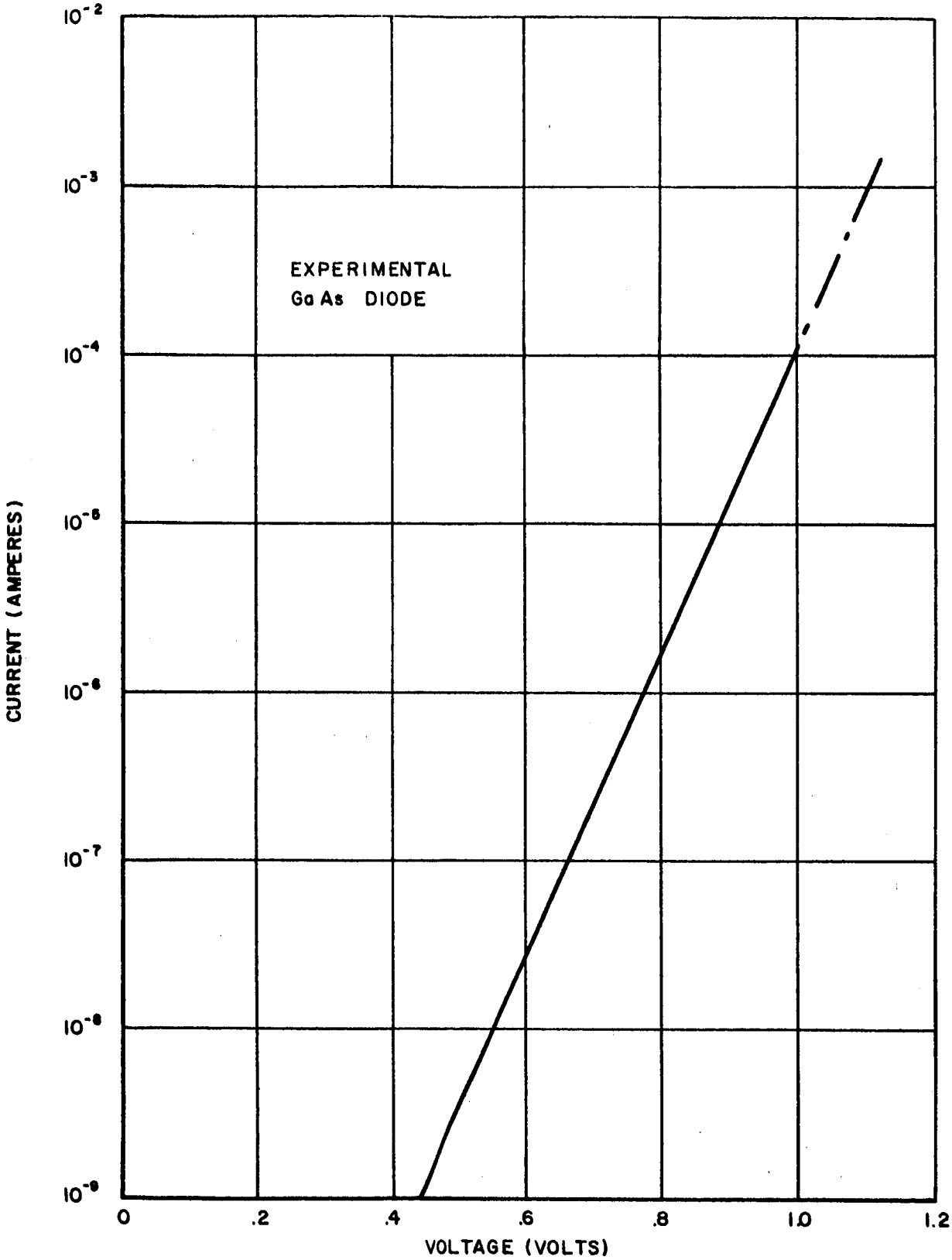
then increased rapidly as the conductance increased, for increasing excitation voltages. Semiconductor theory predicts an experimental rise in capacitance as conduction increases and the measurements with this method agree.

A sheet of silicon diodes formed with boron as the P-type dopant and utilizing a planar passivated process was placed in a specially fabricated test jig. The static characteristics were measured and found to be quite uniform from diode to diode, and similar to the static characteristics of the General Electric unit SSD558.

A more reliable contact to a single diode from the sheet was made with a small drop of conducting epoxy placed on the boron surface. The static characteristics were verified, but the capacitance of this diode as measured with the bridge described above, was 26.3 picofarads at values of low conductance or about 10 times greater than the capacitance of the commercial unit. This single diode was tested in the two line system with a series photoconductor and found to exhibit a low nonlinear ratio.

An improved spring loaded point contact was incorporated in the original test jig to minimize probe capacitance. The static characteristic was similar to the above, but the capacitance remained high at 27.8 pf., indicating a high charge storage in the junction itself, and emphasizing the need to experiment with smaller junction areas.

A silicon diode similar to the General Electric SSD558, but fabricated without the gold doping usually employed, was tested and found to give operating characteristics substantially better than the former. A variety of other diodes have been tried with no better increase in nonlinear action. Among these have been low capacitance varactor diodes. Diodes have been specially fabricated for this project within the Electronics Laboratory. A GaAs diode with low junction capacitance was obtained and found to be extremely nonlinear, yielding a nonlinear ratio of 40 in the equivalent circuit test. The static characteristic is shown in Figure 20. Higher pulse voltages are required to switch the diode



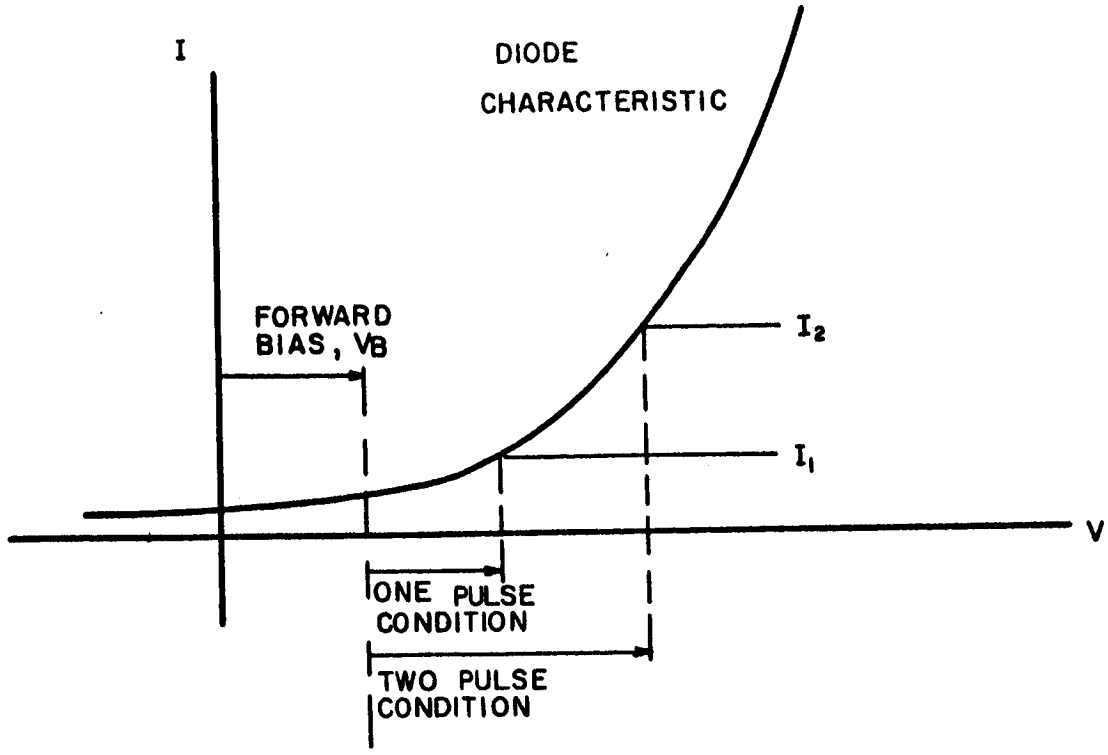
V-I CHARACTERISTICS OF GaAs DIODE

FIGURE 20

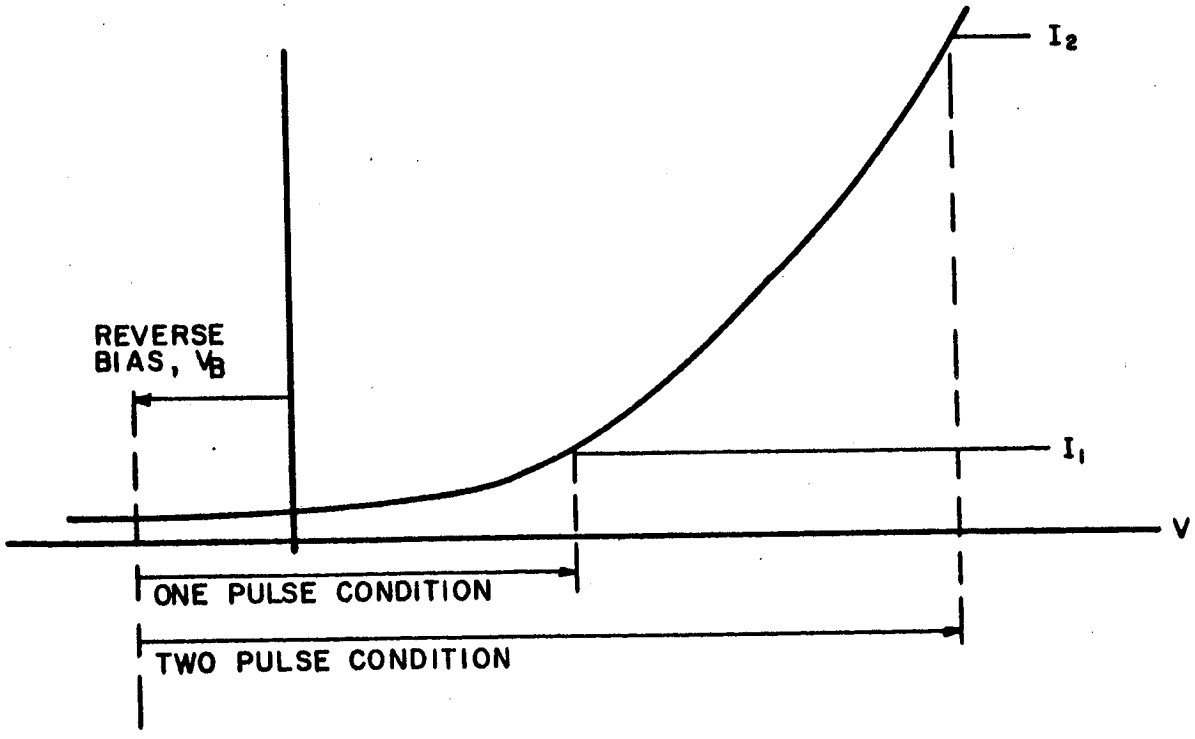
properly, however, because of the higher band gap of the GaAs. This effect can be observed by comparing Figures 16 and 20. Silicon diodes were fabricated also and found to compare favorably with the silicon diode described above.

In an attempt to improve the nonlinear switching ratios, biasing techniques were tried. Theoretically, a small reverse bias on the diode should allow a large pulse voltage to be used, with no increase in conduction for a single pulse, but a much larger conduction for two coincident pulses, as illustrated in Figure 21. The diode capacitance, however, is still a problem and only a very small increase in nonlinear ratio was observed in the actual test.

A second method of enhancing nonlinear action was investigated. This involves the action of a resonant switch now being used in microwave applications. The switching depends upon the nonlinear characteristics of a diode to change from a series to a parallel resonant mode. A representative circuit is shown in Figure 22a. As can be seen in 22b, biasing the diode into conduction will cause the parallel resonant mode of C_1 and L to dominate, presenting a high impedance to the characteristic frequency. On the other hand (Figure 22c), the reversed biased diodes has no affect on the circuit and the low impedance series resonant mode of L and C_2 will dominate. According to calculations, an impedance charge of the order of Q^2 will result. Also the inherent capacitance of the diode can be used to advantage rather than being an undesirable parameter to be minimized. The problems involved in resonating LC combinations at the delay line pulse frequencies, however, are great. The physical size of high Q coils and the necessity to damp the unwanted response as well as the impedance change requirements of the diode, have postponed the application of this method of switching.

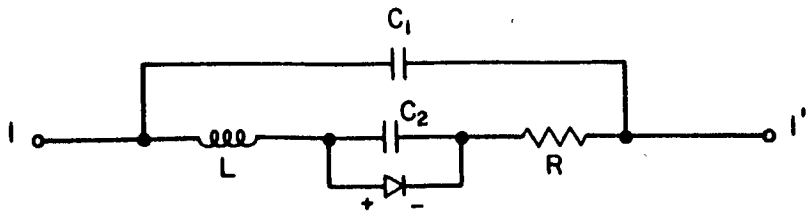


a.) FORWARD BIAS CONDITION

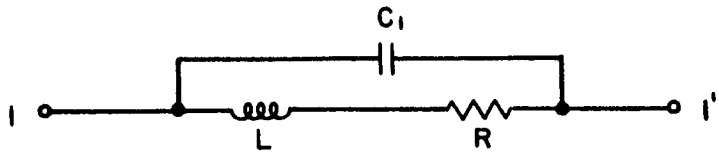


b.) REVERSE BIAS CONDITION

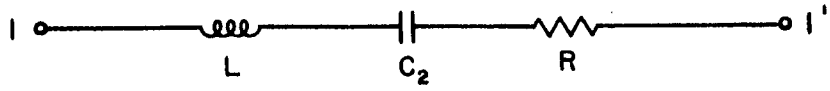
EFFECT OF DIODE BIASING
FIGURE 21



a. EQUIVALENT CIRCUIT



b. PARALLEL RESONANCE (DIODE FORWARD BIASED)



c. SERIES RESONANCE (DIODE REVERSE BIASED)

RESONANT SWITCHING

FIGURE 22

III. PHOTOCONDUCTOR MATERIAL AND REQUIREMENTS

The image is transduced to an electrical quantity in the photoconductor whose resistance is a monotonically decreasing function of the light incident upon its surface. To compare favorably the vidicon, the photoconductor should be sensitive to illumination in the range of .1 to 10 foot candles. To function properly in the image converter, its change in resistance must be transformed accurately into a video signal at the converter output. Once the ideal characteristics are determined, the task of preparing the photoconductor material and geometry begins. Ideally, this video output will be an optimization of high signal-to-noise ratio and good gray scale rendition, consistant with standard image converter requirements.

The problems of delay line selection and nonlinear element switching have been discussed. Referring to the equivalent circuit of Figure 10, the photoconductor requirements can be determined. At low light levels the higher photoconductor impedance will easily dominate the impedance levels of the conducting diode, the load impedance, and the delay line impedances. At higher light levels, however, the photoresistance will be lower but must remain above the remaining circuit impedance for ease of control of the series current. This becomes especially important when shunting effects are considered.

It must be noticed, however, that the extent of diode conduction depends upon the value of the photoresistance so that the output current is not a simple function of the latter. The experimental results of this nonlinearity will be discussed in the next sections.

To help establish the necessary requirements, commercially available photoconductor units were tested in the equivalent circuit. The Clairex CL603AL a CdSe photoconductor was selected because of its success in the equivalent circuit; it has an impedance of approximately 1000 ohms under ambient lighting conditions, and a dark resistance in the megohm region.

Tests were made on photoconductor elements fabricated within the Electronics Laboratory Optoelectronics section. The present configurations of these elements exhibit a higher resistance characteristic than the CL603AL, due primarily to the differences in electrode layout. Improvements in the electrode configuration and the application of transparent electrodes have been studied with the desire to make available, more desirable elements and technology.

The capacitance of the photoconductors becomes important when the device dark resistance is considered. Using the measuring technique previously mentioned in diode testing, the shunt capacitance of the photoconductor elements was determined as 2.7 pf, which is essentially constant, independent of both illumination and the voltage across the element. This capacitance will affect the light characteristic of the photoconductor operating in the pulsed circuitry, but will not be a detrimental factor in the interrogation problem.

The effect of added capacitance across the photoconductor is to increase the signal current through the load by decreasing the total impedance. The extent to which the photoresistance maintains control of the current is demonstrated in the sections that follow.

Along with the discrete element characterization, the problems associated with the deposition of continuous photoconductive layers have been investigated. CdSe was chosen for initial experiments because of its combination of spectral response, response time and sensitivity. Utilizing techniques previously developed to deposit sintered CdSe PC cells on glass substrates, attempts were made to form photoconductive layers on silicon wafers. After spraying the layer, the assembly was sintered and heat treated. Good mechanical contact has been attained and the layers are photoconductive, though extensive testing of their properties has not been undertaken.

Indium is known to make ohmic contact to CdSe and CdS single crystals. Indium electrodes were evaporated upon the previously fabricated CdSe-silicon assemblies and were then electrically evaluated. Though reason-

ably low resistance was attained, the nonlinear dark V-I characteristic showed the contact to be nonohmic. Some chemical reaction between the CdSe and In may have occurred during evaporation. In addition, there remains a problem of depositing sufficient In for low resistance contact without shorting through the PC to the Si wafer.

IV. IMAGE CONVERTER CONFIGURATION

The image converter's operating principles, as they have evolved, have been described in Section I. The characteristics of delay line photoconductor, and nonlinear element, both idealized and actual, have also been presented. Before the actual configuration of the image converter can be determined, however, the question of how the system is to be scanned, or interrogated must be asked. When a workable system has been generated and its elemental intersections are specified, then the exact shunting effect of the non-interrogated elements can be determined.

Scanning - In the conventional television system, the image is scanned from left to right, top to bottom, in a sequence of interlaced, horizontal lines. Because the image focused on our matrix is optically reversed, the scan must proceed from left to right and bottom to top, when viewed from the front. Consider the diagram of Figure 23. Two delay lines are shown schematically connected to the conductor matrix. The delay line tap voltages have been "timed" so that the first (bottom) line of the tilted image area will be scanned. The series combination of diode and photoconductor are shown on this line in Figure 23 as circles.

Consider now the scanning of the second line with the intersections marked with crosses. To accomplish this, the "y" delay line voltage must be delayed one tap and the "x" line voltage advanced one tap, with respect to their timing in Figure 23. For this scan to occur immediately following the scan of the first line, a pulse must be initiated on delay line "y" during the first scan. In fact, there are necessarily two pulses on both delay lines at any instant in time, since a similar situation exists with delay line "x". To prevent any cross-interaction between these sets of pulses, it is necessary to eliminate elements from some of the intersections, as Figure 23 has shown. The pulses are then timed so that an even-even and an odd-odd correspondence in output taps accomplishes the scanning of the total image area. It must be noted, of course, that the matrix shown in Figure 23 can be expanded to include more elements; the scanning principle remains the same. The retriggering of the drive pulses can be timed from the delay line tap outputs.

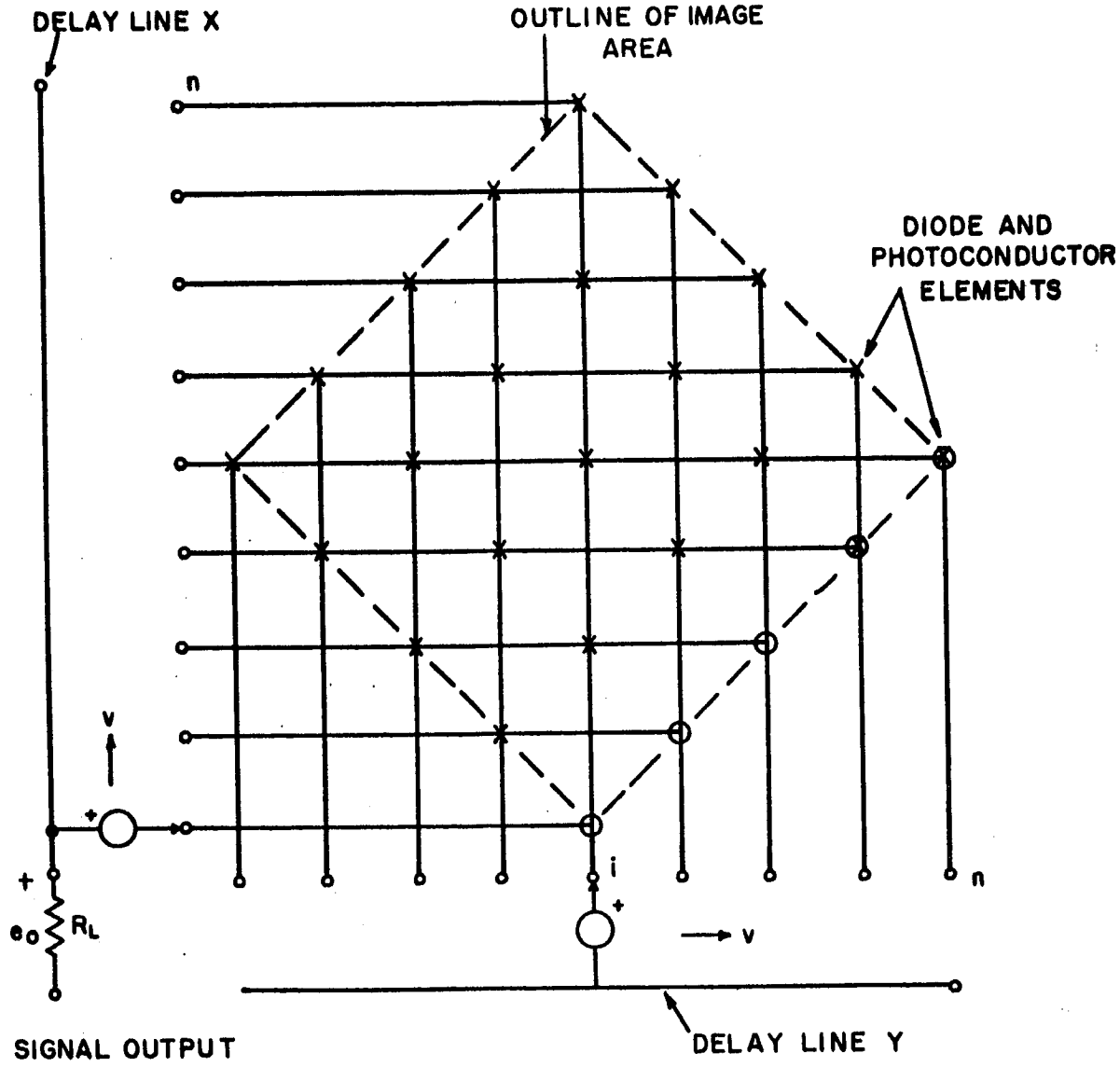


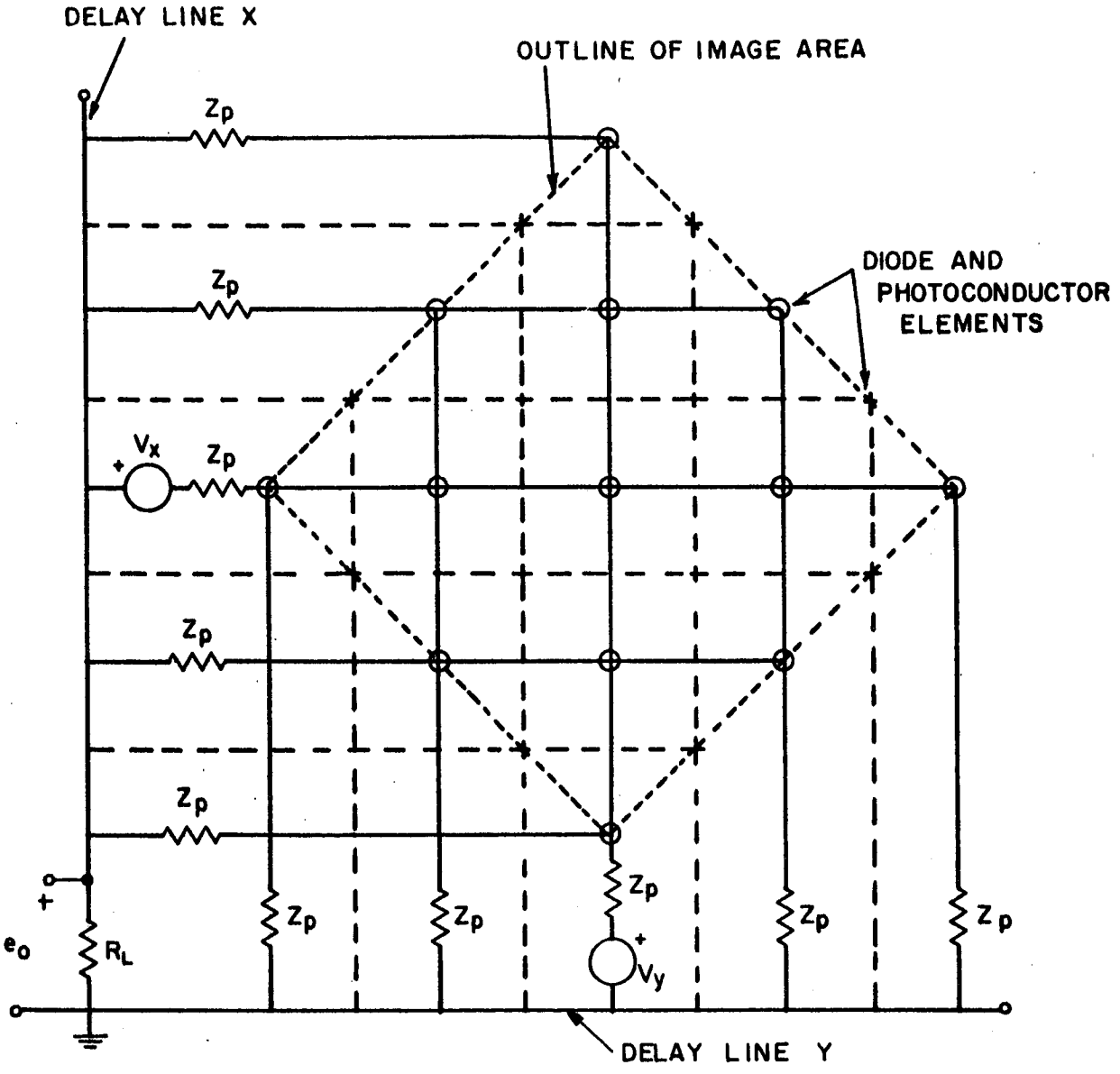
IMAGE CONVERTER MATRIX SCANNING
FIGURE 23

Matrix Shunting Effects - Once the configuration of the matrix has been established, the problems in interrogation can be investigated. Figure 24 shows the matrix of Figure 23 when the center element is interrogated.* The desired signal path is the series circuit of center element, both pulse voltage sources, and the load resistor, as has been shown in Figure 10. Other elements, however, are directly attached to this interrogation circuit; these are shown as circles in Figure 24. The elements in the major diagonals contribute the most undesirable shunting; these elements have a single pulse voltage across them and, therefore, have an unavoidable conductance. The Thevenin equivalent impedance of the delay line, Z_p, is also shown; this impedance includes the constant output pad described previously. The remaining circles elements shunt signal current between the delay line impedance and the diagonal lines.

The remaining elements of the matrix are shown as crossed intersections. It is evident that there is no direct interconnection between this section of the matrix and the interrogated element, and that its effect is simply to shunt the load resistor, R_L. The voltage across these elements, then, will never be greater than the signal voltage, and their conduction will be less severe than the previous elements described.

It is now quite evident why the conduction of the noninterrogated elements must be minimized to reduce shunting. In order to facilitate the specification of elemental conductance characteristics, the equivalent circuit of Figure 25 was derived. The impedance Z_1 represents the interrogated element. The impedance Z_2 represents the noninterrogated element impedance. The letter n represents the number of elements per scanning line; e.g., n = 5, in Figure 23 and 24. The crossing impedances in Figure 25 represent the diagonal shunting elements described above; their shunting effect is inversely proportional to (n-1). The diagonal cross-coupling shunt and the load impedance shunt both vary inversely as n^2, and represent the

*This condition represents the "worse case" interrogation, and was therefore chosen for analysis.



SCHEMATIC OF INTERROGATED MATRIX

FIGURE 24

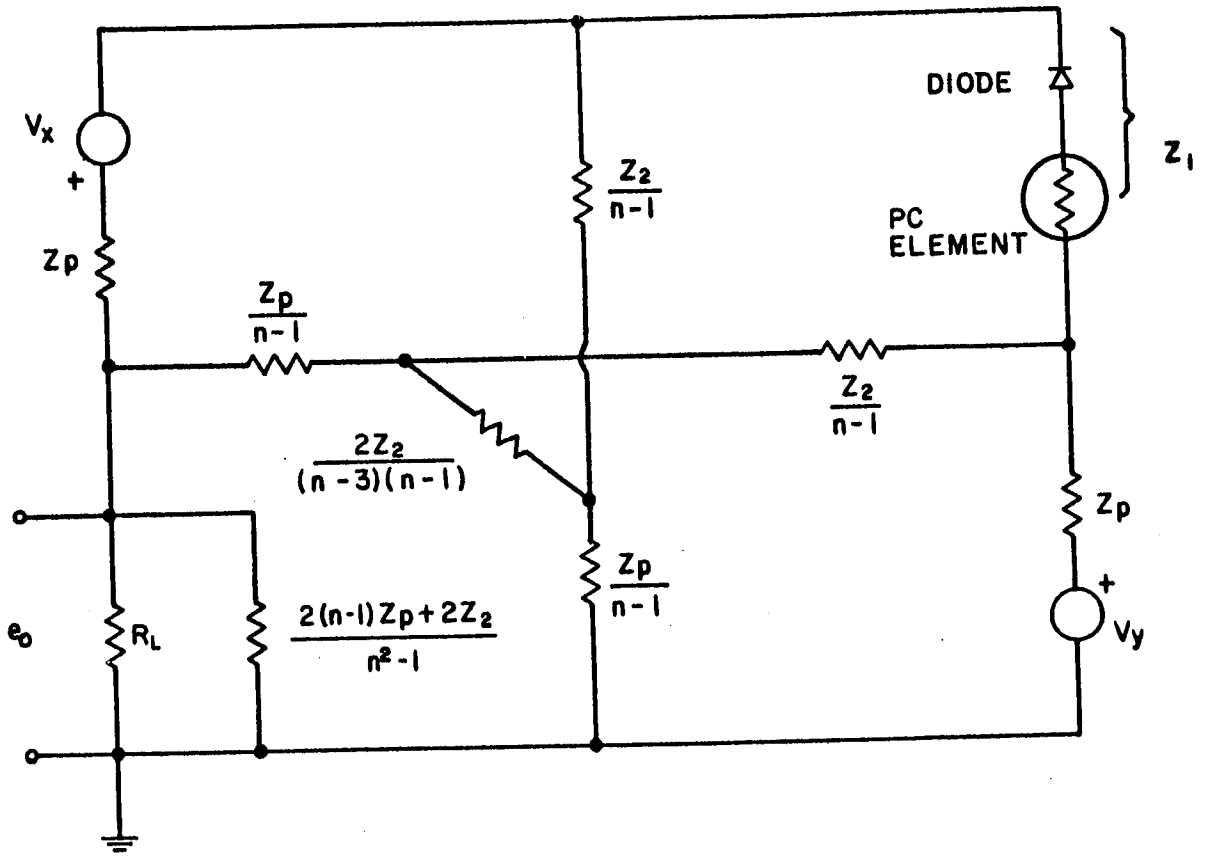


IMAGE CONVERTER EQUIVALENT CIRCUIT

FIGURE 25

remaining circled elements and the crossed elements, respectively, shown in Figure 24. The mathematical justification for this equivalent circuit is given in Appendix II of this report.

Before this equivalent circuit was derived during the program, the simpler, but applicable circuit of Figure 26 had been analyzed. This circuit behaves much like the previous one, if the load resistor value is modified and if $Z_p \ll Z_2$. The matrix solution for output voltage is obtained by striaght-forward circuit analysis and is

$$E_o = \frac{\begin{vmatrix} -\frac{1}{Z_p} & -\frac{n-1}{Z_2} & \frac{V_x}{Z_p} \\ -(\frac{1}{Z_1} + \beta) & \frac{1}{Z_1} & \frac{V_y}{Z_p} \\ -\frac{1}{Z_1}\beta + \frac{1}{Z_1} & & \frac{V_y}{Z_p} \end{vmatrix}}{\begin{vmatrix} -\frac{1}{Z_p} & -\frac{n-1}{Z_2} & \frac{1}{Z_2} + \beta \\ -(\frac{1}{Z_1} + \beta) & \frac{1}{Z_1} & \frac{1}{Z_p} \\ -\frac{1}{Z_1} & \beta + \frac{1}{Z_1} & \frac{n-1}{Z_2} \end{vmatrix}}$$

where $\beta = \left(\frac{1}{Z_p} + \frac{n-1}{Z_2} \right)$

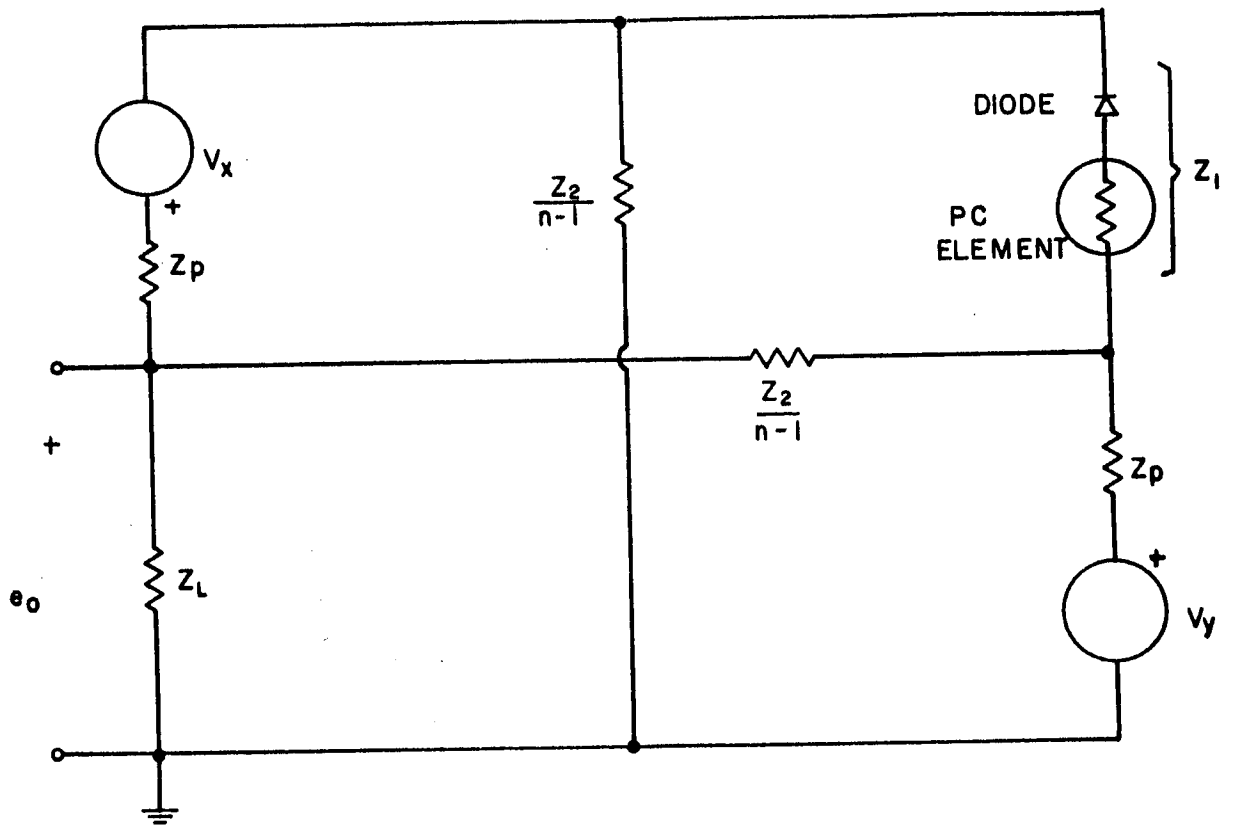
This equation then, expresses the output signal as a function of the significant circuit impedances, and the pulse voltages. The ability of the interrogated impedance, Z_1, to affect a change in the output current can be investigated most easily by assuming constant values of the other parameters and plotting the relationship of E_o and Z_1. This has been done in Figure 27, for the following circuit values:

$$Z_p = 10^2 \text{ ohms } Z_2 = 10^5 \text{ ohms } n = 100 \; Z_L = 10 \text{ ohms}$$

$$V_x = V_z = 1 \text{ volt}$$

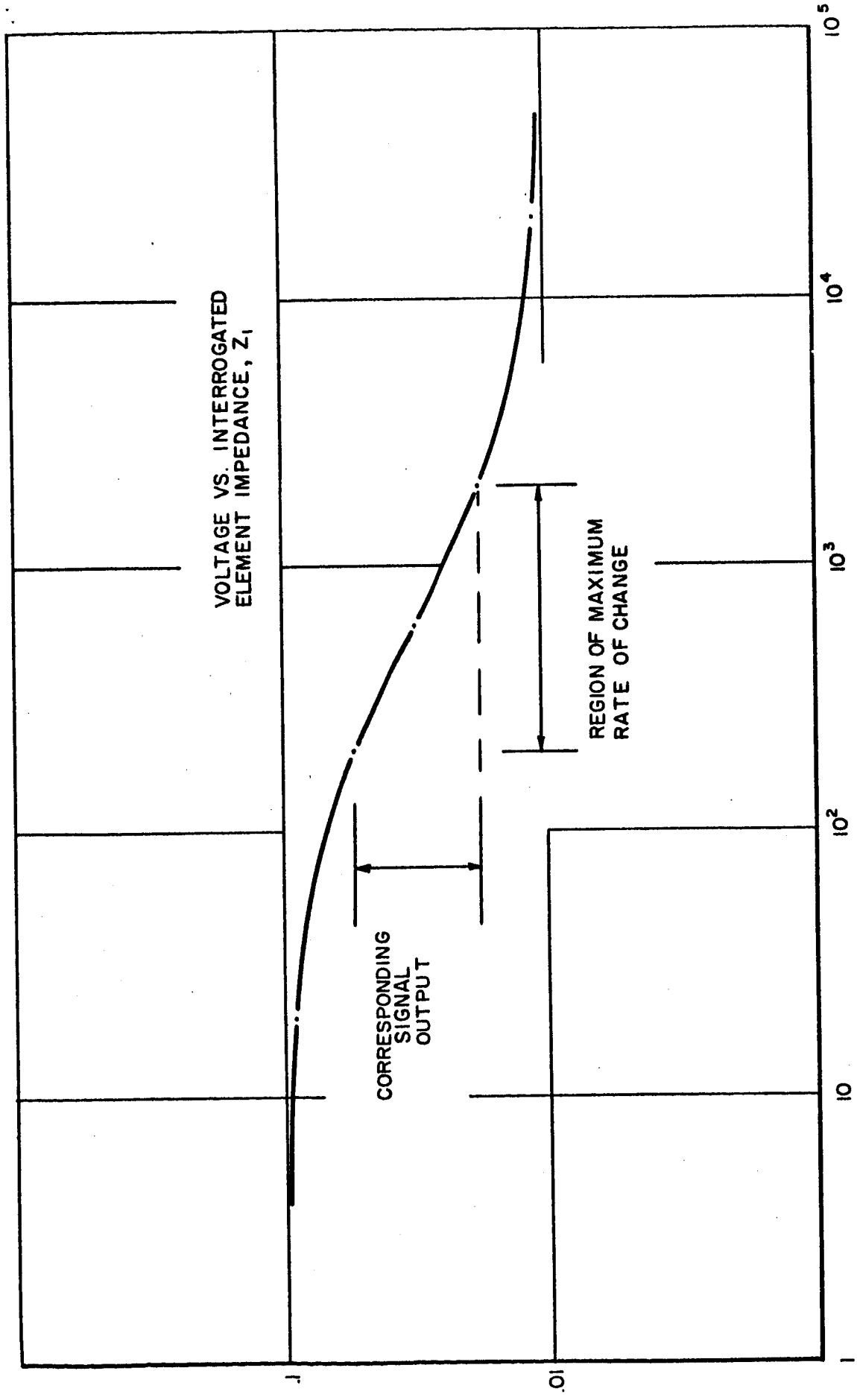
In this case, the above determinants reduce to:

$$E_o = \frac{1}{100} \quad \frac{Z_1 + 2000}{Z_1 + 200}$$



SIMPLIFIED EQUIVALENT CIRCUIT

FIGURE 26



CALCULATED MATRIX CHARACTERISTIC

FIGURE 27

The curve shows the optimum operating impedance for the photoconductor and the series diode, for these particular parameter values; and the corresponding output voltage.

For a lower value of the noninterrogated impedance, $Z_2 = 10^4$ ohms, and no change in the remaining parameters, the image converter fails to properly perform its function. The output voltage becomes:

$$E_o = 1/10 \cdot \frac{Z_1 + 100}{Z_1 + 100} = 1/10$$

which has no functional relationship with Z_1.
This and further plots have given rise to the requirement that:

$$\frac{1}{Z_p} \geq \frac{10\ n}{Z_2} \quad \text{for successful converter operation.}$$

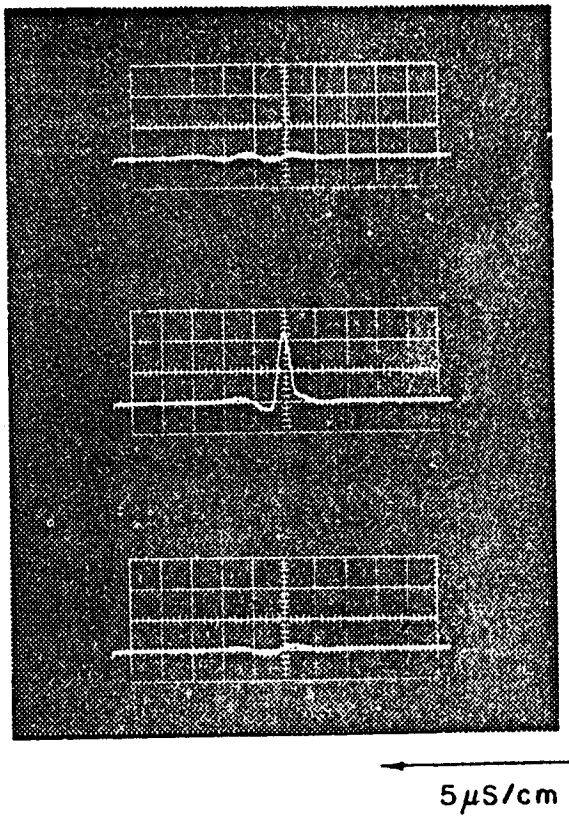
This is equivalent to suggesting that the maximum number of elements per line, or lines per frame (in a square matrix) is:

$n \leq \frac{Z_2}{10\ Z_p}$, dependent upon the maximum value of Z_2 and the minimum value of Z_p.

Experimental Results - The first experiments, after the initial selection of the tapped delay line described previously, were concerned with a single element series circuit, as has been shown schematically in Figure 10. The two ten-tap ceramic delay lines, driven by standard pulse generators, served as the pulse voltage sources to evaluate the single element photoconductors and diodes. From the variety of elements tested, the first notable result was obtained with a General Electric SSD 558 silicon diode and the Clairex CL603AL photoelement. An oscilloscope photograph of the output voltage, for pulse coincidence and non-coincidence, with and without illumination, is shown in Figure 28. The nonlinear ratio, or the ratio of interrogated to non-interrogated output, was $\frac{44.\ mv}{2.5\ mv} = 17.6$. This is necessarily lower than the ratio calculated in Section I, because of the larger value of series photoresistance and because of capacitive shunting of the diode. This test circuit was also used in the evaluation of the fabricated diodes and for further photoconductor selection.

The next significant demonstration was the construction and operation of a nine element image converter, utilizing three taps of each delay line, as illustrated in Figure 9. This model uses the elemental combination tested

SINGLE ELEMENT



SINGLE ELEMENT INTERROGATION, USING 2 DELAY LINES, NON-LINEAR ELEMENT & PHOTO-CONDUCTIVE ELEMENT.

FIGURE 28

above--the GE SSD558 diode and the Clairex CL603AL photoconductor--at each intersection. The operation of this model is demonstrated by the photograph of Figure 29. The dependence of each video output pulse on both the illumination and on the coincidence condition is clearly shown. The nonlinear ratio has degraded noticeably over that of Figure 28, due again to the shunting effect of the non-interrogated elements; its value is $\frac{40 \text{ mv}}{5 \text{ mv}} = 8$. This figure, however, represents a reduction of only slightly more than two, for the addition of eight elements, further evidence that no single element is directly in parallel with an interrogated element.

To investigate the shunting effect experimentally, the schematic of Figure 26 was built and tested. The values of the shunting branch parameters were varied to determine the change in output signal. Figure 30 shows the results of this equivalent circuit test for the following element values:

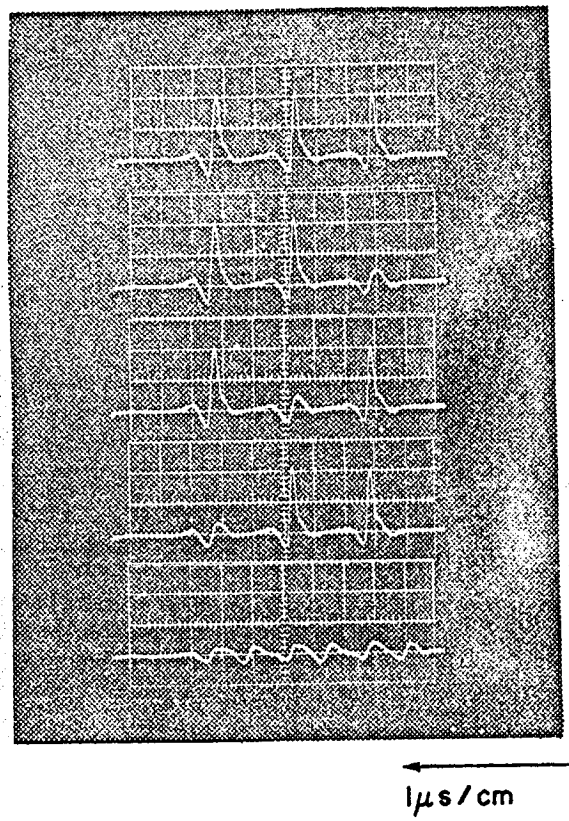
Z_p = 1500 pf and 330 ohms in parallel

$\frac{Z_2}{n-1}$ = 100 pf

Z_L = 110 ohms

The photoconductor used is the Clairex CL603 AL, with 2000 pf of shunt capacity added. The diode used is the silicon unit fabricated without gold doping. The signal obtained with peak illumination is 320 mv, although the nonlinear ratio is low, as expected. The significance of this experiment now depends upon the values of Z_2 that can be obtained. For a diode shunt capacity of 3.3 pf, which can easily be obtained, the test functions as the equivalent of a 30 x 30 matrix. For lower diode capacitance, the value of n will increase, although the signal output voltage will decrease, due to a decrease in Z_L.

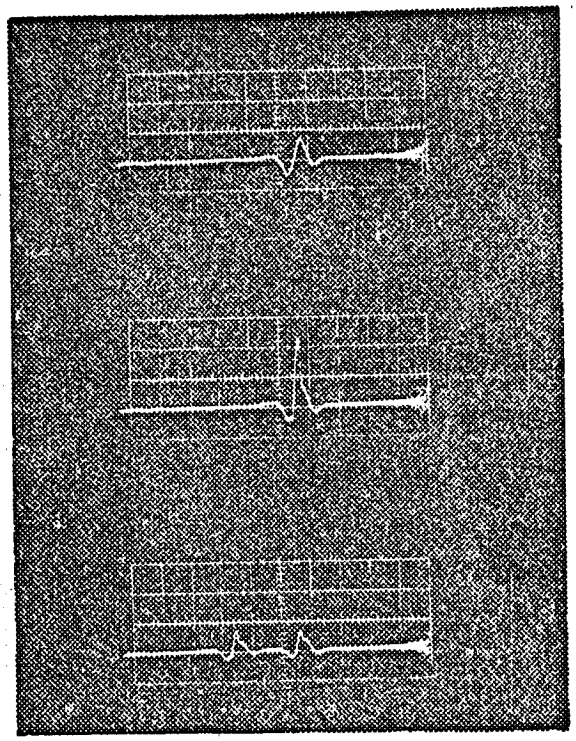
The transfer characteristic of the same circuit is shown in Figure 31. This characteristic was obtained with a calibrated electroluminescent source electrically isolated from the converter, in contact with the photoconductor, and with the elements enclosed in a light-tight test box to exclude ambient lighting. The initial portion of the curve is quite linear, but higher illumination levels yield less signal output. It is to be noted, however, that



NINE ELEMENT ARRAY, CONNECTED TO TWO DELAY LINES, WITH 9 NON-LINEAR ELEMENTS & 9 PHOTO-CONDUCTIVE ELEMENTS.

FIGURE 29

"N" ELEMENT ARRAY



A. COINCIDENT PULSES.
NO ILLUMINATION
(PEAK VOLTAGE, 140 mV)

B. COINCIDENT PULSES.
ILLUMINATED ELEMENT.
(PEAK VOLTAGE, 460 mV.)

C. NON-COINCIDENT PULSES.
ILLUMINATED ELEMENT.
(THRESHOLD VOLTAGE, 140 mV)

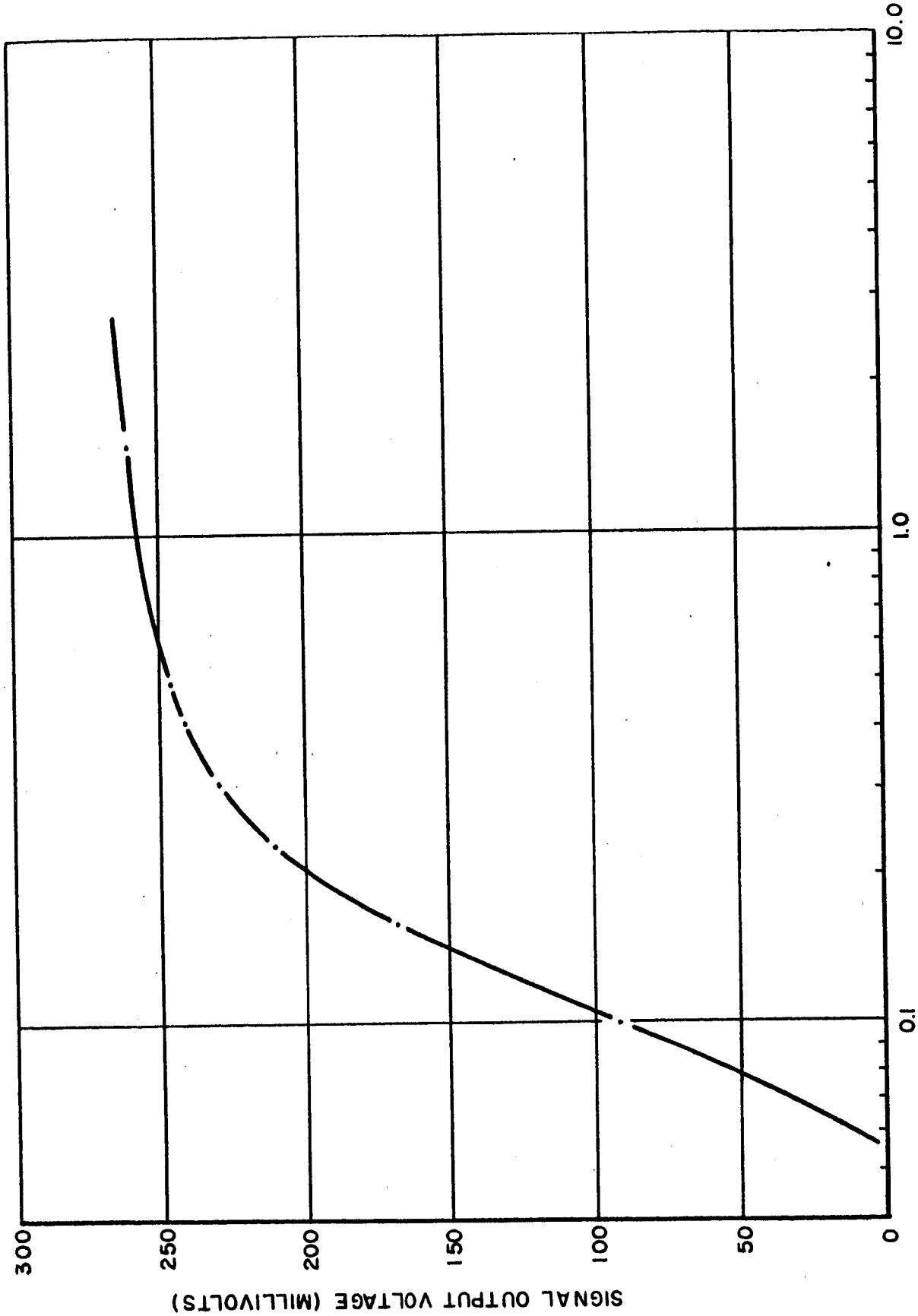
200
mV/cm

1μ5/cm

EFFECTIVE SIGNAL = 320 mV

"N" ELEMENT INTERROGATION, WITH SHUNTING OF ARRAY SIMULATED BY EQUIVALENT CIRCUIT.

FIGURE 30



TRANSFER CHARACTERISTIC OF UNCOMPENSATED IMAGE CONVERTER CIRCUITRY

FIGURE 31

diode conduction and photoconductor resistance play a large part in determining the characteristic; then interaction can be controlled, and a more linear curve obtained, if required.

The success of this test is due largely to the effect of increased photoconductor capacitance. This addition has caused an increase in voltage across the diode and therefore the larger values of forward conduction, which has offset the conduction of the shunt branches.

RECOMMENDATIONS

The initial progress on the image converter mode during this contract strongly suggests that continuing efforts in this direction will be rewarding. It is suggested that an effort be made in the semiconductor materials area to obtain arrays of diodes with suitable characteristics and interconnections. An effort in the photoconductor materials area is needed to obtain arrays of interconnected photoconductive elements, with the proper transfer characteristics. The matching of diode and photoconductor characteristics can be obtained with equivalent circuit techniques. Further development of delay line devices should be aimed at obtaining an optimization of line length and pulse output, with uniform characteristics from tap to tap.

As larger arrays are developed, a precise determination of the pulse drive requirements and the video amplifier specification can be undertaken. The construction of a prototype as these tasks are completed will allow a direct evaluation of the optical and electrical functioning and structure within the environment of operation.

APPENDIX I

Love Waves

The use of a thin layer of ceramic supported by a thick substrate as a scanning delay line was investigated during this program. Two cases were considered. First, the thin ceramic would be polarized in the thickness direction and propagate longitudinal elastic waves. In the second case, the ceramic would be polarized through its width and propagate shear waves. Both cases represent wave propagation in a layered structure and have been extensively studied in connection with seismographic theory.* The analysis of longitudinal waves is rather complicated and will not be given here. However, since the shear wave case is more concisely presented and is characterized by a slower velocity of propagation, it will be reproduced here. The purpose of this analysis is to derive the period equation for shear waves in a thin layer underlain by a solid half space, so-called love waves. Figure 32 shows the notation for this discussion. Here a layer of thickness H is shown on an infinitely thick substrate. The origin of the coordinate axis is taken at the interface, with the x axis in the direction of propagation and the z axis vertically downward. It is assumed that all displacements are independent of the y coordinate and that all time variations are sinusoidal.

Assuming solutions consisting of horizontally polarized shear waves with displacements V_1 and V_2 in the y direction, we can write for these displacements

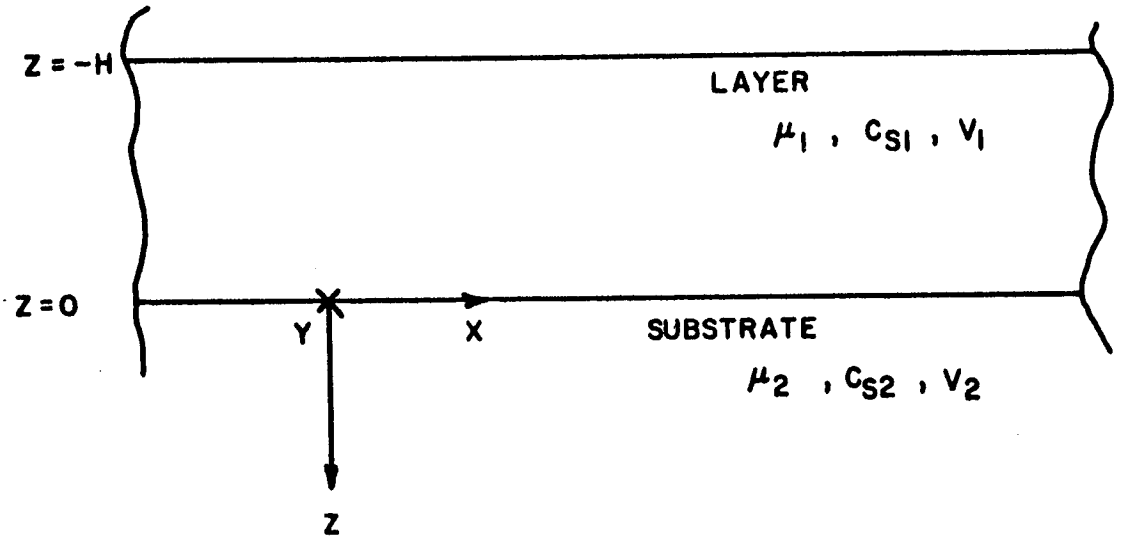
$$V_1 = (Ae^{iK\gamma_1 z} + Be^{-K\gamma_1 z})\, e^{-iK(x-ct)}$$

in the layer, and

$$V_2 = C\, e^{iK(-\gamma_2 z - x + ct)}$$

in the substrate.

*"Elastic Waves in Layered Media," Ewing, Jardetsky and Press, McGraw-Hill, 1957.



LAYER UNDERLAIN BY A SOLID HALF SPACE

FIGURE 32

In these equations,

$$\gamma_1 = \sqrt{\frac{c^2}{c_{s1}^2} - 1} \quad ,$$

$$\gamma_2 = \sqrt{\frac{c^2}{c_{s2}^2} - 1} \quad ,$$

$$c_{s1} = \sqrt{\frac{\mu_1}{\rho_1}} \quad ,$$

$$c_{s2} = \sqrt{\frac{\mu_2}{\rho_2}} \quad ,$$

and

$$K = \frac{\omega}{c} = \frac{2\pi f}{c} \quad ,$$

where c is phase velocity, c_s is shear wave velocity, ρ is the density, and μ is the shear modulus. A, B, and C are constants determined by the boundary conditions, which require that the stress p_{zy} vanish at the free surface and be continuous, together with the displacement at the interface. The boundary conditions on $p_{zy}\Big|_{Z=-H} = \mu \frac{\partial v}{\partial z} = 0 =$

$$\underset{Ae^{-K\gamma_1 H}}{} \quad \underset{- Be^{iK\gamma_1 H}}{}$$

and

$$(p_{xy})_1\Big|_{z=0} = (p_{xy})_2\Big|_{z=0} = \mu_1 \gamma_1 (A-B) = -\mu_2 \gamma_2 C \quad .$$

The continuity of displacement at the interface requires that

$$V_1\Big|_{z=0} = V_2\Big|_{z=0} = A + B = C \quad .$$

Finally, these conditions on A, B, and C can be grouped together:

$$
\begin{array}{lll}
A\, e^{-iK\gamma_1 H} & -B\, e^{iK\gamma_1 H} & = 0 \\
A\,\mu_1\gamma_1 & -B\,\mu_1\gamma_1 + C\mu_2\gamma_2 & = 0 \\
A & +B \qquad -C & = 0 \,.
\end{array}
$$

The system of equations will have solutions different from zero if

$$
\Delta = \begin{vmatrix} e^{iK\gamma_1 H} & -e^{iK\gamma_1 H} & 0 \\ \mu_1\gamma_1 & -\mu_1\gamma_1 & \mu_2\gamma_2 \\ 1 & 1 & -1 \end{vmatrix} = 0 \,,
$$

or

$$
\tan (K\gamma_1 H) = \frac{\mu_2}{\mu_1} \sqrt{\frac{1 - c^2/c_{s2}^2}{c^2/c_{s1}^2 - 1}} \,.
$$

This period equation may be put in a more convenient form by defining a normalizing frequency f_o as the frequency at which the later thickness is one wavelength at the shear velocity of the material,

$$
f_o \, H = c_{s1}
$$

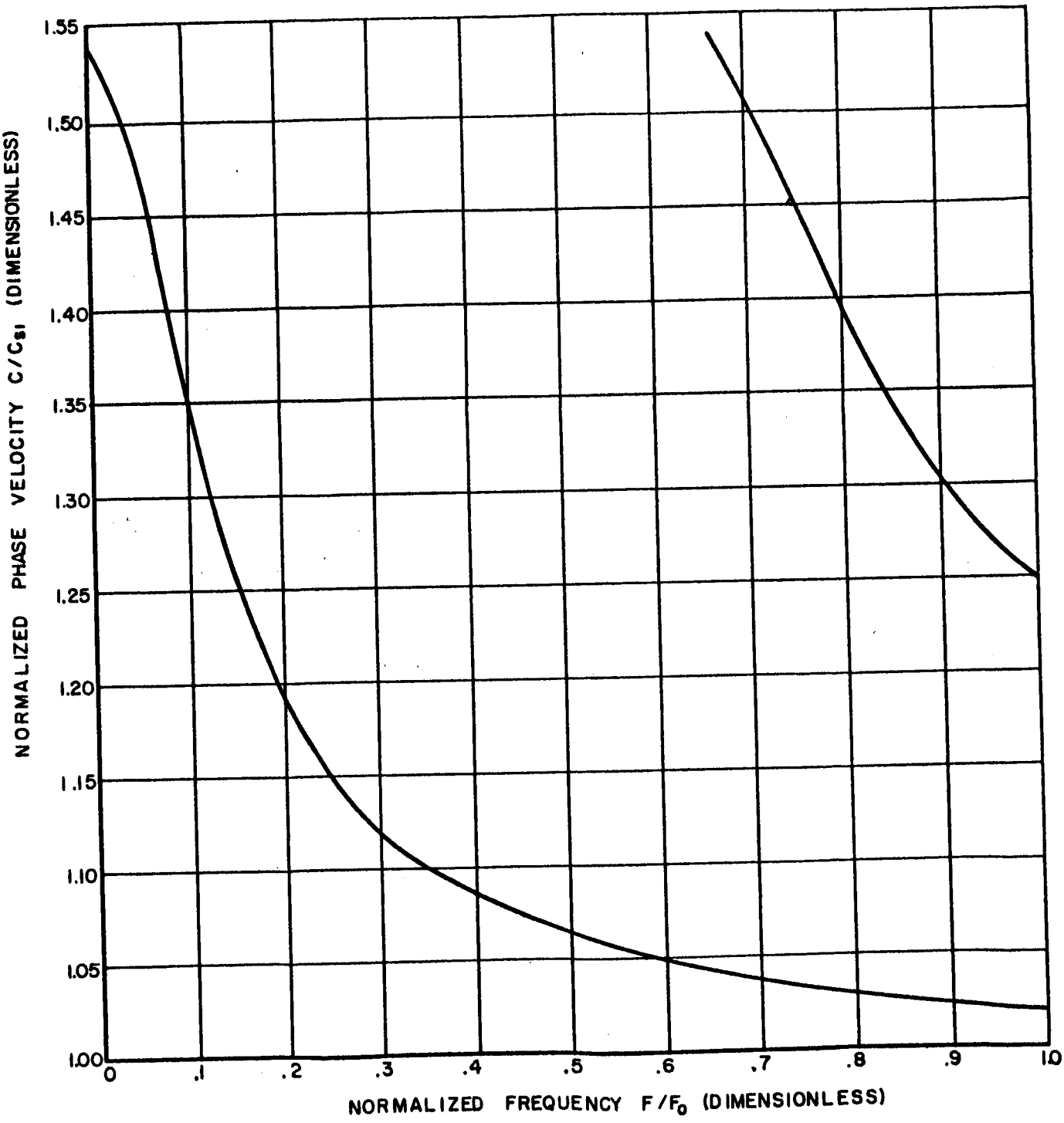
or

$$
f_o = \frac{c_{s1}}{H} \,.
$$

Using this, and noting that $\mu = \rho c_s^2$ in each material, the period equation can be written as

$$
\tanh \left(2\pi \frac{f/f_o}{c/c_{s1}} \sqrt{1 - \frac{c^2}{c_{s1}^2}}\right) = -\frac{\rho_2}{\rho_1} \frac{c_{s2}^2}{c_{s1}^2} \sqrt{\frac{1 - c^2/c_{s2}^2}{1 - c^2/c_{s1}^2}}
$$

$$
= -n^2 \frac{\rho_2}{\rho_1} \sqrt{\frac{1 - \dfrac{c^2/c_{s1}^2}{n^2}}{1 - c^2/c_{s1}^2}} \,,
$$



PHASE VELOCITY VS. FREQUENCY FOR CERAMIC SHEET ON ALUMINUM SUBSTRATE.

FIGURE 33

where $n = \frac{c_{s2}}{c_{s1}}$.

Figure 33 shows the solution of this equation for the case of a lead zirconate titanate ceramic layer on an aluminum substrate. It may be seen that acoustic dispersion is quite severe, so that distortion of an acoustic pulse will occur unless the ceramic thickness is much less than an acoustic wavelength. It was for this reason that this configuration was not pursued further during this program.

APPENDIX II

Circuit Analysis of Interrogated Matrix

A diagrammatic layout of the image converter matrix has been shown in Figure 24. To aid in understanding the converter operation and in specifying the element characteristics, this matrix has been transformed to the equivalent circuit of Figure 25 and 26, by making appropriate approximations. The following pages will outline the method pursued and justify the simplifications that were made.

The center element in Figure 24 is assumed to be the interrogated element, since this interrogation includes the two longest diagonal conductors in direct connection, and is therefore the worse case interrogation. As explained previously, the "crossed elements" are to be considered separately, since they are not directly connected to the circled elements. Although the figure shows a 5 x 5 matrix, the equivalent circuit will be derived for the general case.

The first transformation to be made is merely that of rearrangement. Figure 34 shows a matrix, which although larger than the matrix of Figure 24 (9 x 9), is basically the same form, redrawn. The following elements can be identified:

Z_1 = the interrogated element impedance.

Z_p = the Thevenin equivalent delay line output impedance, including resistor pads.

V_x, V_y = the delay line output voltage.

Z_L = the load impedance, to include the shunting of the "crossed element" matrix.

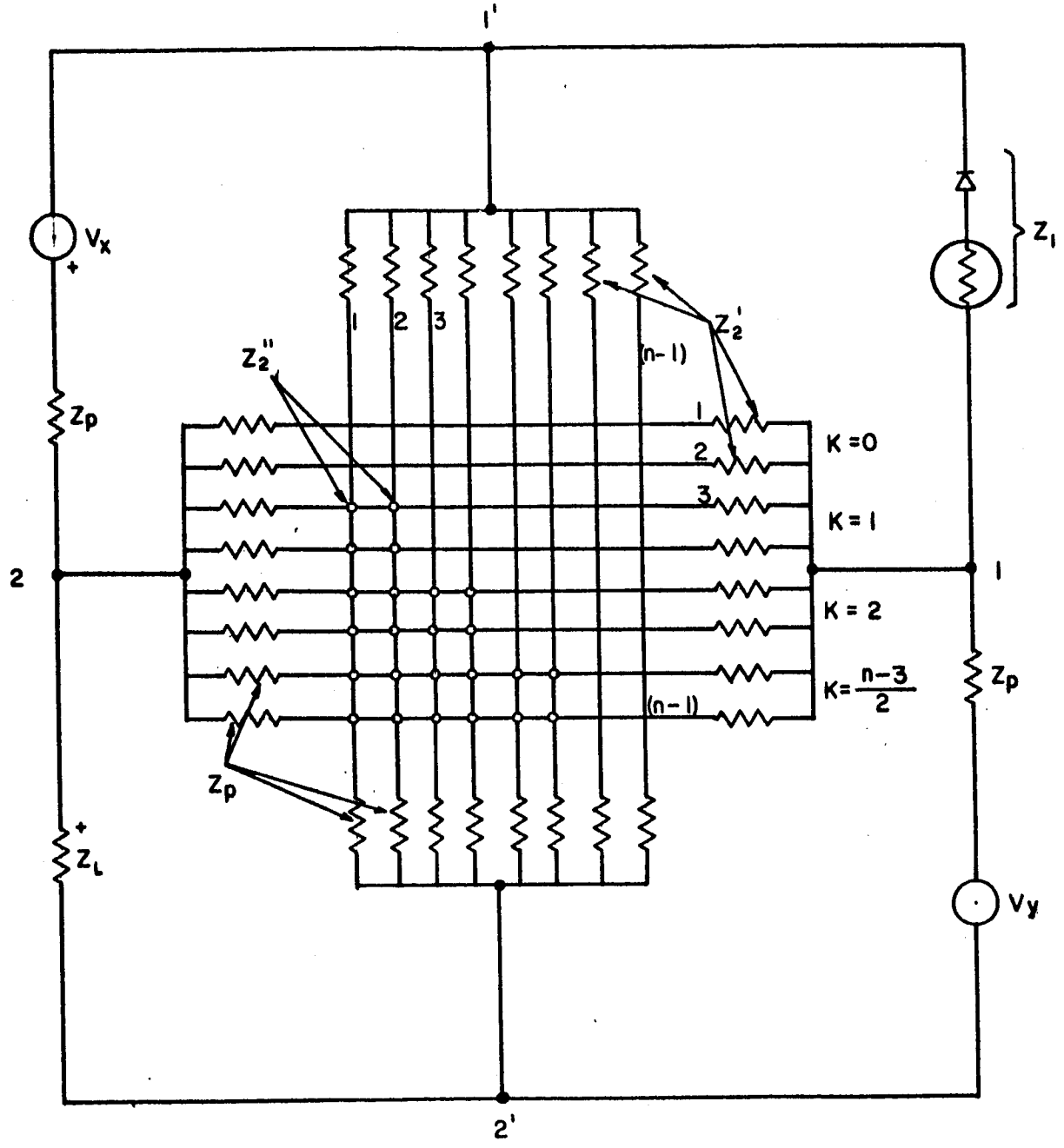
Z_2' = the noninterrogated element impedances, which are found in the two longest diagonal conductors.

Z_2'' = all other noninterrogated element impedances.

Comparing Figures 24 and 34, the following discoveries are made:

1) There are two sets of (n-1) Z_2' impedances, each set with a common connection (4 in the 5 x 5 matrix, 8 in the 9 x 9 matrix).

2) There are two sets of (n-1) Z_p impedances, each set opposite and connected to a Z_2' set, with the other side in a common connection.



TRANSFORMED MATRIX ARRAY

FIGURE 34

3) There are $\frac{(n-3)(n-1)}{2}$ Z_2'' impedances, interconnecting these two sets at the junction of Z_p and Z_2. (4 in the 5 x 5 matrix, 24 in the 9 x 9 matrix).

4) There will be $\frac{n^2-1}{2}$ "crossed elements" (12 in the 5 x 5 matrix, 40 in the 9 x 9 matrix), and two sets of (n-1) Z_p impedances, interconnected across the load impedance.

Assume now (without justification) that the vertical junction conductors in Figure 34 are all at one potential and the horizontal junction conductors are all at a second potential. With this assumption, the two sets of conductors become parallel conducting planes. The impedances that are now in parallel are combined into one impedance as follows:

1) The Z_2' sets become impedances of $\frac{Z_2}{n-1}$.

2) The Z_p " " " " $\frac{Z_p}{n-1}$.

3) The Z_2'' set becomes an impedance of $\frac{2Z_2}{(n-3)(n-1)}$

The "crossed element" matrix is to be considered in the same manner, as if its parallel conductors were conducting planes. The Z_2'' impedances of this submatrix becomes a lumped impedance of $\frac{2Z_2}{n^2-1}$ in series with 2 sets of $\frac{Z_p}{n-1}$ impedances. The total impedance becomes:

$$Z = \frac{2Z_2}{n-1} + \frac{2Z_2}{n^2-1} = \frac{2(n+1)\,Z_p + 2Z_2}{n^2 - 1}$$

These impedance values are precisely the values of Figure 25; the equivalent circuit has been obtained. The task of justifying the "conducting plane" assumption remains, to complete the proof, however.

The difference between this solution and a second solution, where only the vertical conductors in Figure 34 are considered as one conducting plane will now be investigated. The character of this difference will yield information about the accuracy of our first solution.

The single conducting plane assumption will allow the following simplifications:

1) The upper set of Z_2' impedances become $\frac{Z_2}{r-1}$

2) The lower " " Z_p " " $\frac{Z_p}{n-1}$

3) The horizontal impedances of Z_p, Z_2'', and Z_2' may be grouped in pairs to obtain "T" networks. There will be $\frac{n-3}{2}$ of these "T" networks, plus the first "degenerate" T, an impedance of $\frac{Z_p + Z_2}{2}$.

The T networks can now be transformed to Pi networks, and the circuit will appear as in Figure 35a. To simplify this transformation, the T networks are numbered from k = 1 to k = $\frac{n-3}{2}$. Each T network has arm impedances of $\frac{Z_p}{2}$ and $\frac{Z_2}{2}$, and a leg impedance of $\frac{Z_2}{4K}$. Applying the Wye-Delta network transformations, the impedances of Figure 35a are found to be:

$$Z_1 = \frac{Z_2}{4K\, Z_p}\left[(1 + 2K)\, Z_p + Z_2\right]$$

$$Z_2 = \frac{1}{4K}\left[(1 + 2K)\, Z_p + Z_2\right]$$

$$Z_3 = \frac{1}{2}\left[(1 + 2K)\, Z_p + Z_2\right], \text{ for } K = 1,2,\ldots\frac{n-3}{2}$$

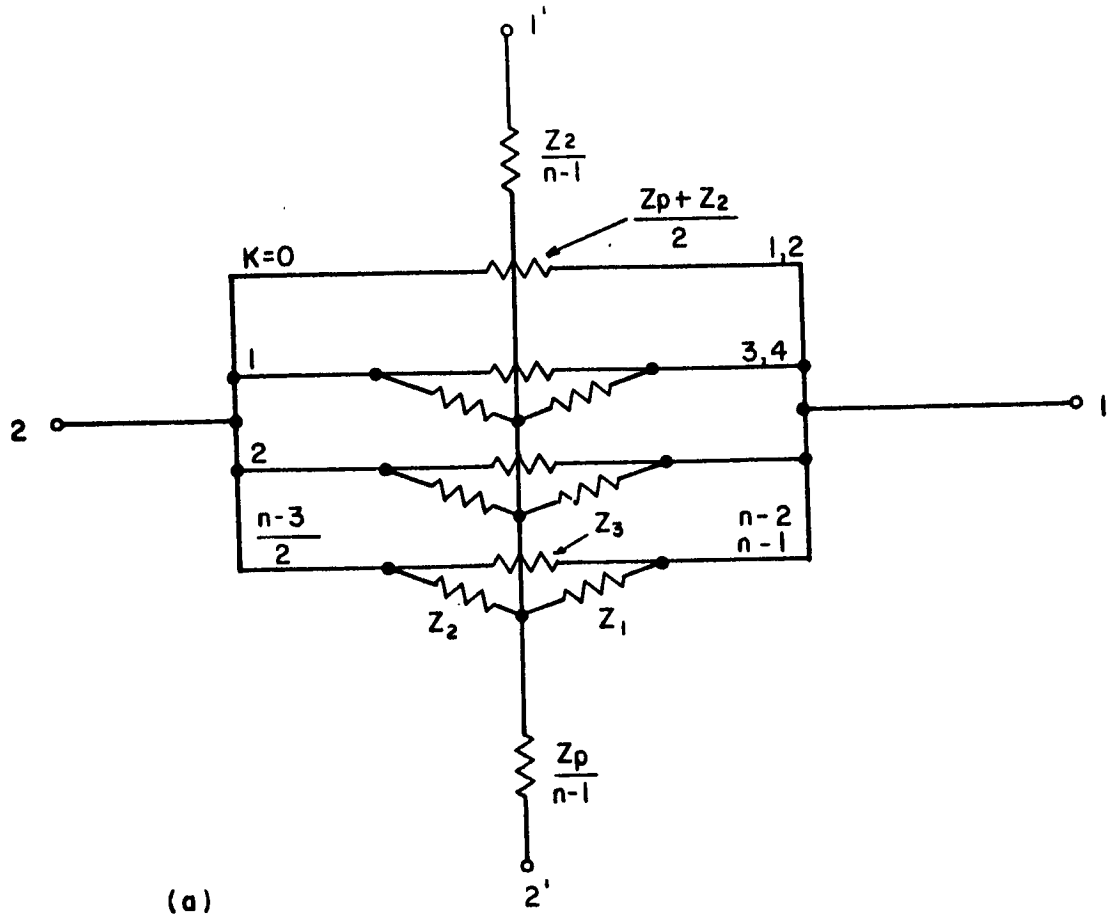
To obtain Figure 35b, the impedances in parallel must be combined. The admittance from 1-2,

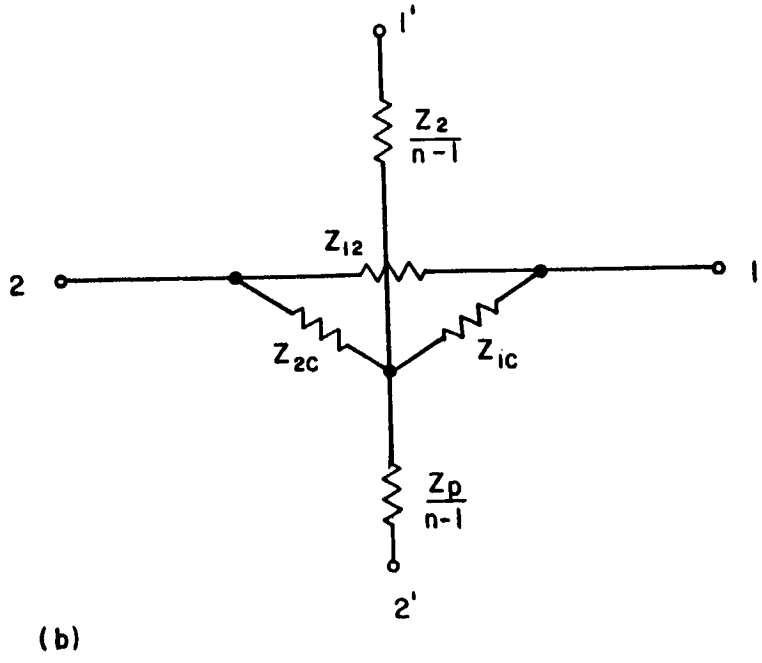
$$Y_{12} = \frac{2}{Z_2+Z_p} + \sum_{K=0}^{K} \frac{2}{(1+2K)Z_p + Z_2}$$

$$= \sum_{K=0}^{K} \frac{2}{(1+2K)Z_p + Z_2} = \frac{1}{Z_p} \sum_{k=0}^{k} \frac{1}{K + \beta}$$

where $\beta = \frac{1}{2}\left[1 + \frac{Z_2}{Z_p}\right]$

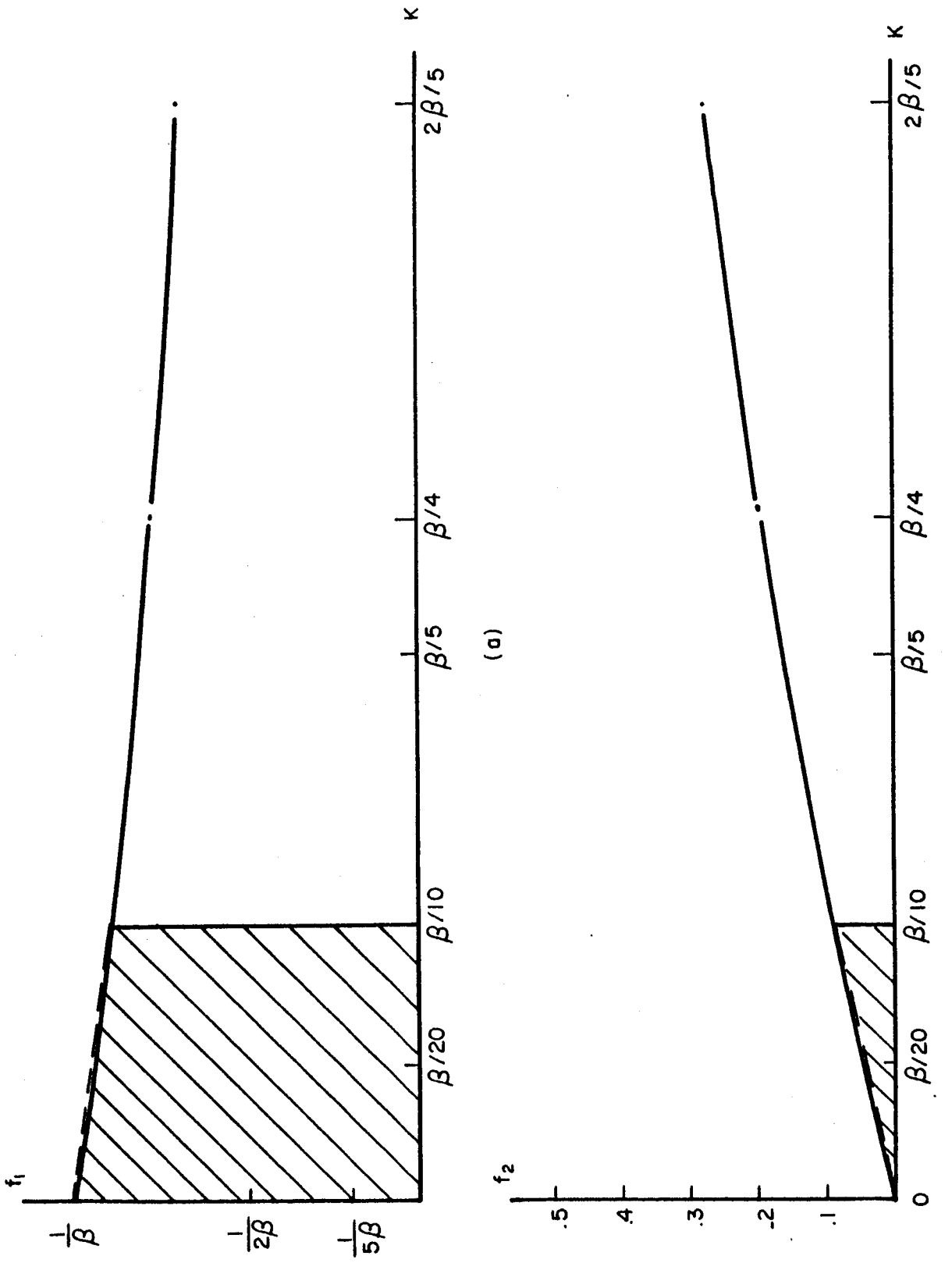
If the expected values are substituted for Z_2 and Z_p from Section III, $\beta \simeq 500$. Therefore, for n = 100, K $\simeq$ 50, and the summation above can be approximated by a graphical integration, illustrated in Figure 36a. In this





IMPEDANCE TRANSFORMATIONS

FIGURE 35



GRAPHICAL APPROXIMATION
FIGURE 36

figure, $f_1 = \frac{1}{\beta+K}$ is plotted as K. There will be little error for reasonable values of n.

Therefore,

$$Y_{12} = \frac{1}{Z_p} \sum_{K=0}^{K} \frac{1}{K+\beta} = \frac{K+1}{K/2+\beta}$$

and, $Z_{12} = \frac{1}{Y_{12}} = \frac{1}{2}\left(Z_p + \frac{Z_2}{K+1}\right) = \frac{1}{2(n-1)}\left[Z_p(n-1) + {}_2Z_2\right]$.

Similarly, the second admittance, Y_{2c}, may be found using graphical approximation.

$$Y_{2c} = \sum_{K=1}^{K} \frac{4K}{(1+2K)Z_p + Z_2} = \frac{2}{Z_p} \sum_{K=1}^{K} \frac{1}{1+\beta/K}$$

where $\beta = \frac{1}{2}\left(1 + \frac{Z_2}{Z_p}\right)$.

In Figure 36b, $F_2 + \frac{1}{1+\beta/K}$ is plotted versus K, and the area for n = 100 is considered. Again, the linear approximation is made, and

$$Y_{2c} = \frac{2}{Z_p} \sum_{K=1}^{K} \frac{1}{1+\beta/K} = \frac{2}{Z_p} \frac{K'}{1+2\beta/K}$$

$$\text{so, } Z_{2c} = \frac{1}{Y_{2c}} = \frac{Z_p(K+1) + Z_2}{2K^2} = \frac{Z_p(n-1) + {}_2Z_2}{(n-3)^2}$$

An inspection of the equations for Z_1 and Z_2 will indicate that:

$Z_1 = \left(\frac{Z_2}{Z_p}\right) Z_2$.

$$\text{so, } Z_{1c} = \frac{Z_2\left[Z_p(n-1) + {}_2Z_2\right]}{Z_p \cdot (n-3)^2}$$

To simplify these three equations, let $R = Z_p(n-1) + 2Z_2$.

Then,

$$Z_{12} = \frac{R}{2(n-1)}$$

$$Z_{2c} = \frac{R}{(n-3)^2}$$

$$Z_{1c} = \frac{R\,Z_2}{Z_p(n-3)^2}$$

One more Delta-Wye transformation is necessary, to obtain the circuit of Figure 25. Applying the transformation,

$$Z_a = \frac{Z_{12}\, Z_{2c}}{Z_{12} + Z_{2c} + Z_{1c}} = \frac{R^2 Z_2}{R\left[\frac{1}{2(n-1)} + \frac{1}{(n-3)^2} + \frac{1}{Z_p(n-3)^2}\right]}$$

Finally,

$$Z_a = \frac{Z_p}{n-1} \left[\frac{R}{Z_p N + 2Z_2} \right]$$

$$\text{where } N = \frac{(n-3)^2}{n-1} + 2$$

Similarly, $Z_b = \frac{Z_2}{n-1} \cdot \left[\frac{R}{Z_p N + 2 Z_2} \right]$

and $Z_c \cdot \frac{2Z_2}{(n-3)(n-1)} \cdot \left[\frac{n-1}{n-3} \right] \cdot \left[\frac{R}{Z_p N + 2 Z_2} \right]$

These are precisely the values that were obtained by the first method of analysis, except for the bracketed factors. However, for the previously suggested values of the variables:

$$Z_p = 100, \quad Z_2 = 10^5 \qquad n = 100 ,$$

The bracketed factors are very close to unity, and the impedance values become:

$$Z_n = \frac{Z_p}{n-1} \qquad Z_c = \frac{2 Z_3}{(n-3)^2}$$

$$Z_b = \frac{Z_2}{n-1}$$

The first solution then, appears to be quite accurate, and justifies the use of the equivalent circuit of Figure 25.